Intel Enterprise Processors Technology

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Agenda

- Intel Architecture in Enterprise
- Intel® Xeon™ Processor MP
- Next Generation Intel® Itanium™ Processor
- Interconnect Technology
- Summary

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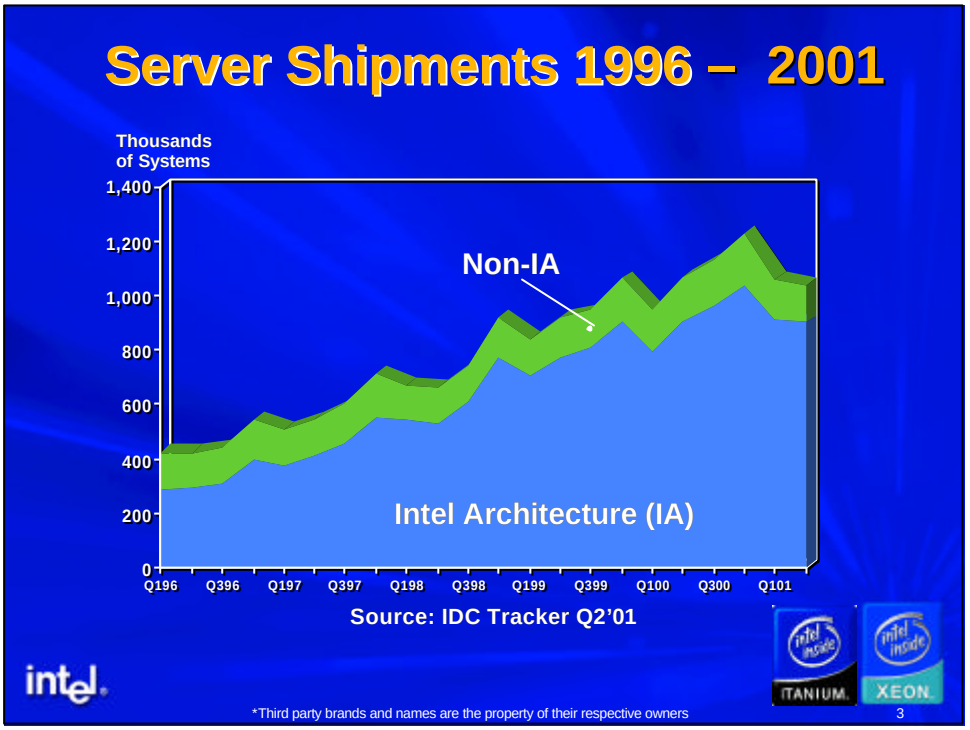
Server Shipments 1996 – 2001
Thousands of Systems
1,400
1,200
1,000
800
600
400
200
0
Non-IA
Intel Architecture (IA)
Q196
Q396
Q197
Q397
Q198
Q398
Q199
Q399
Q100
Q300
Q101
Source: IDC Tracker Q2'01
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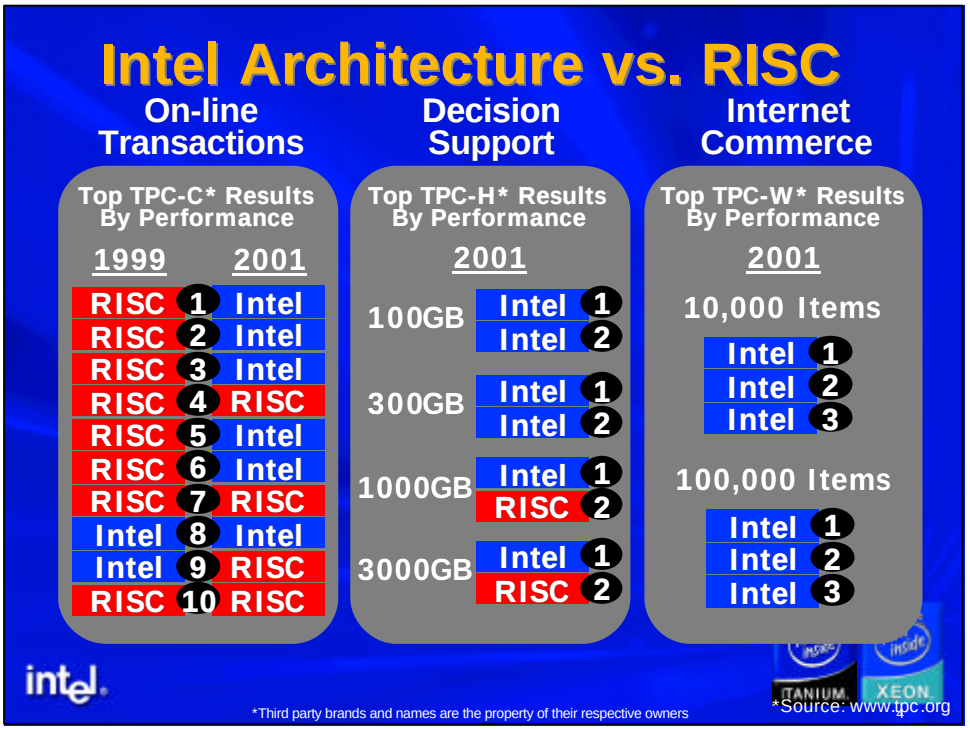
Intel Architecture vs. RISC
On-line Transactions
Top TPC-C* Results By Performance
1999
2001
RISC 1 Intel
RISC 2 Intel
RISC 3 Intel
RISC 4 RISC
RISC 5 Intel
RISC 6 Intel
RISC 7 RISC
Intel 8 Intel
Intel 9 RISC
RISC 10 RISC
Decision Support
Top TPC-H* Results By Performance
2001
100GB
Intel 1
Intel 2
300GB
Intel 1
Intel 2
1000GB
Intel 1
RISC 2
3000GB
Intel 1
RISC 2
Internet Commerce
Top TPC-W* Results By Performance
2001
10,000 Items
Intel 1
Intel 2
Intel 3
100,000 Items
Intel 1
Intel 2
Intel 3
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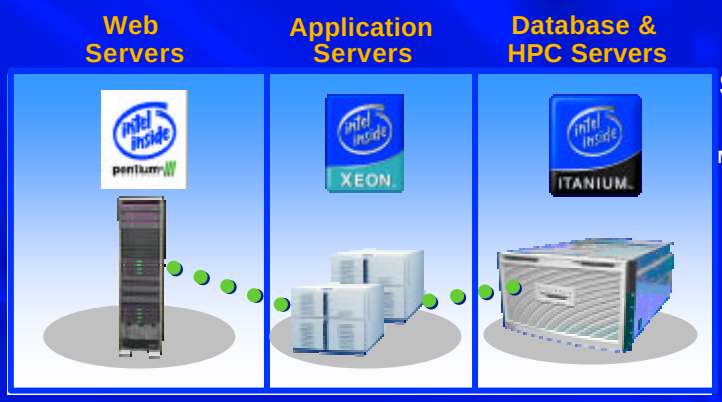
*Source: www.tpc.org

Flexibility for Enterprise and Scientific Environments



Introducing the new Intel® Xeon™ Processor

Intel® Xeon™ Processor MP

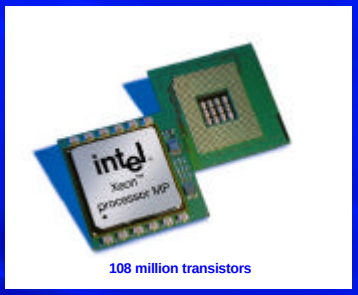
Features for Multi-Processor Server Platforms

Integrated Three Level Cache
1MB or 512KB Level 3 Cache
+ Level 2 Advanced Transfer Cache 256KB

400MHz System Bus

Speeds up to 1.60 GHz

Intel® NetBurst™ Microarchitecture



108 million transistors

144 New SSE-2 Instructions

Hyper-Threading Technology

ServerWorks* Chipset with DDR 200 Memory and PCI-X support

System Manageability Bus

Designed for 4-way, 8-way and above Multi-Processor Servers

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Intel® NetBurst™ Micro-architecture

Delivering new Server capabilities…

400 MHz System Bus — Higher throughput when accessing memory and I/O devices for improved server headroom and scalability

Rapid Execution Engine — 2x clock speed for integer computations providing increased performance for web and database servers

Hyper Pipelined Technology — Higher clock speeds and greater throughput for server workloads resulting in higher transaction rates and faster response times

Streaming SIMD Extensions 2 — New instructions improve response times for media servers, secure transactions and next generation web services

Intel® NetBurst™ micro-architecture enables higher transaction rates and faster response times for new capabilities

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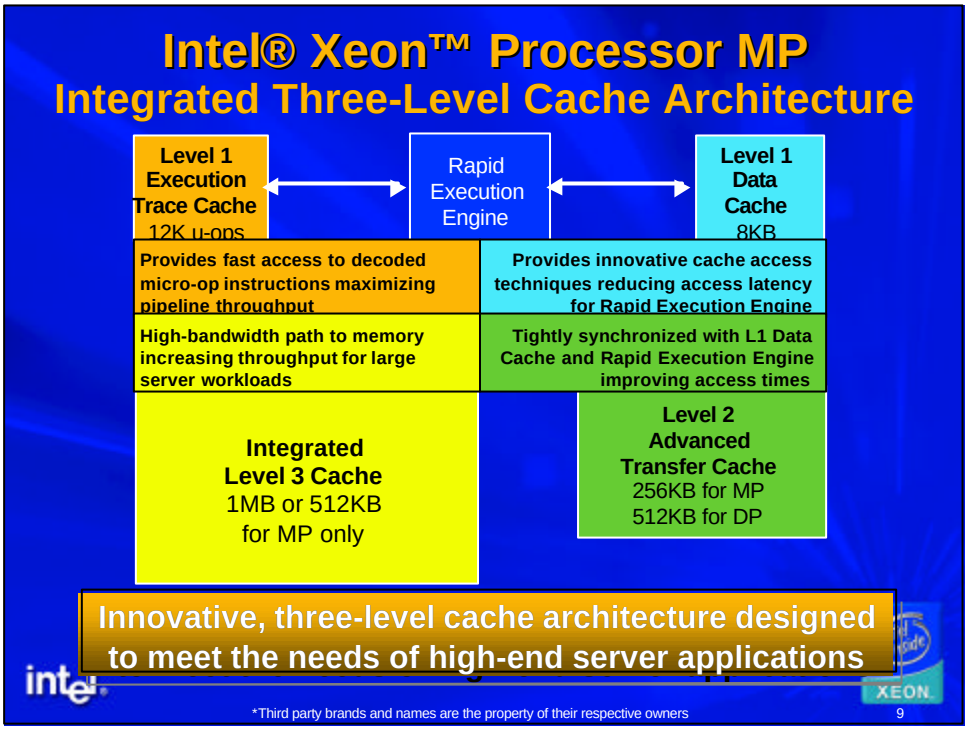
Intel® Xeon™ Processor MP
Integrated Three-Level Cache Architecture
Level 1 Execution Trace Cache
12K µ-ops
Rapid Execution Engine
Level 1 Data Cache
8KB
Provides fast access to decoded micro-op instructions maximizing pipeline throughput
Provides innovative cache access techniques reducing access latency for Rapid Execution Engine
High-bandwidth path to memory increasing throughput for large server workloads
Tightly synchronized with L1 Data Cache and Rapid Execution Engine improving access times
Integrated Level 3 Cache
1MB or 512KB
for MP only
Level 2 Advanced Transfer Cache
256KB for MP
512KB for DP
Innovative, three-level cache architecture designed to meet the needs of high-end server applications
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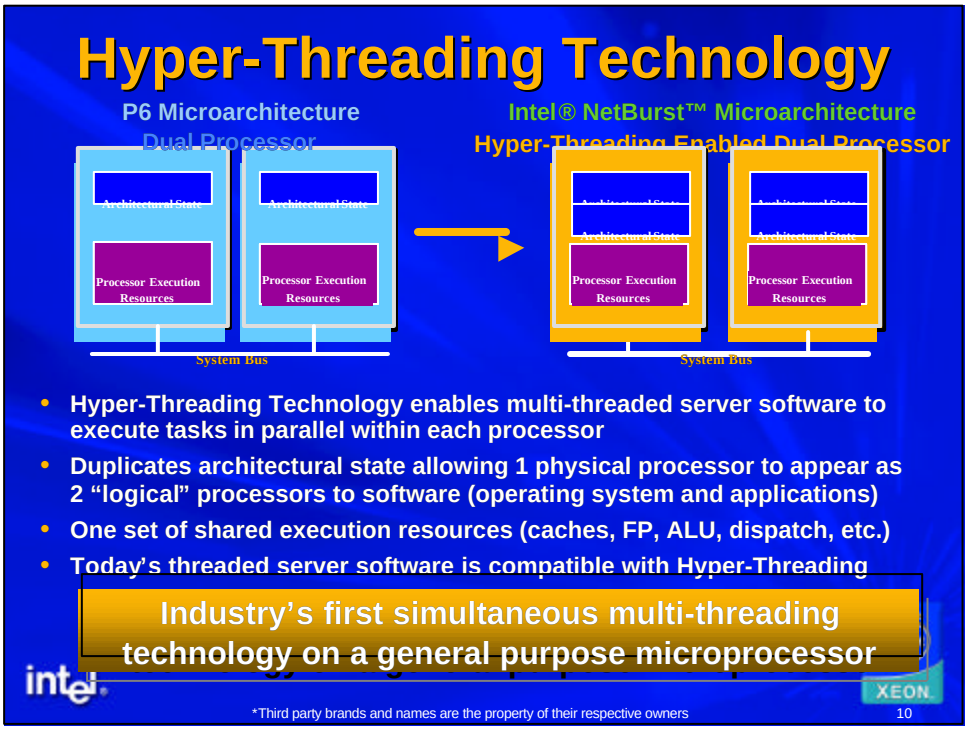
Hyper-Threading Technology
P6 Microarchitecture
Dual Processor
Intel® NetBurst™ Microarchitecture
Hyper-Threading Enabled Dual Processor
Architectural State
Processor Execution Resources
System Bus
• Hyper-Threading Technology enables multi-threaded server software to execute tasks in parallel within each processor
• Duplicates architectural state allowing 1 physical processor to appear as 2 "logical" processors to software (operating system and applications)
• One set of shared execution resources (caches, FP, ALU, dispatch, etc.)
• Today's threaded server software is compatible with Hyper-Threading
Industry's first simultaneous multi-threading technology on a general purpose microprocessor
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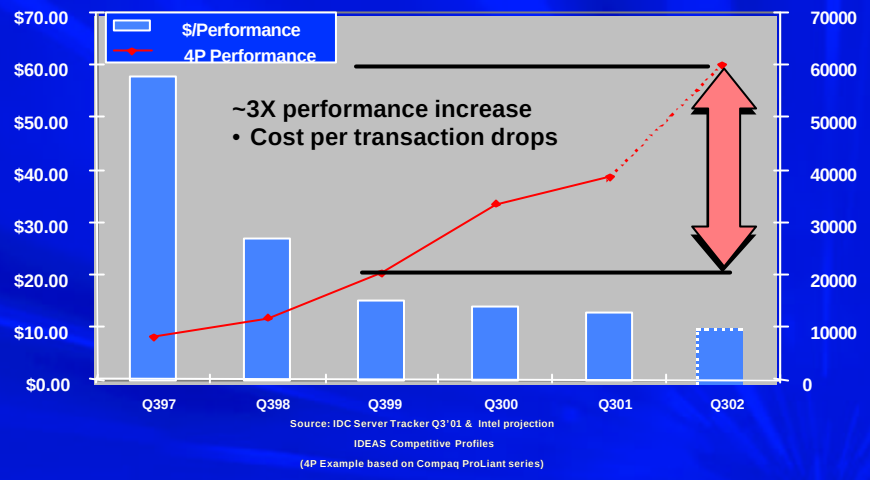
Historical Performance for MP



Source: IDC Server Tracker Q3'01 & Intel projection
IDEAS Competitive Profiles
(4P Example based on Compaq ProLiant series)

Significant installed base of platforms 98-'00 – results in 2-3X performance increase

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Introducing the next generation Intel® Itanium™ Processor

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McKinley Update

- McKinley on schedule for release in mid-2002
  - Sampling to OEMs since Feb '01
  - Pre-production pilot systems underway with end users

- McKinley builds on and extends Itanium™ architecture
  - Improved data speed and throughput
  - Additional execution resources for higher levels of parallelism
  - Compatible with Itanium-based software
- Estimate McKinley to deliver ~1.5-2X performance increase over Itanium-based systems

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EPIC Architecture Features

Explicitly Parallel Instruction Computing

- Performance through parallelism
  - Focused on maximizing instructions executed in parallel
  - Multiple execution units and issue ports in parallel
  - 2 bundles (up to 6 Instructions) dispatched every cycle
- Massive on-chip resources
  - 128 general registers, 128 floating point registers
  - 64 predicate registers, 8 branch registers
  - Provides compiler flexibility to exploit parallelism
  - Efficient management engines (register stack engine)
- Scalable
  - Modular, able to seamlessly add execution resources, issue ports

Architecture designed to maximize synergy of compiler and hardware

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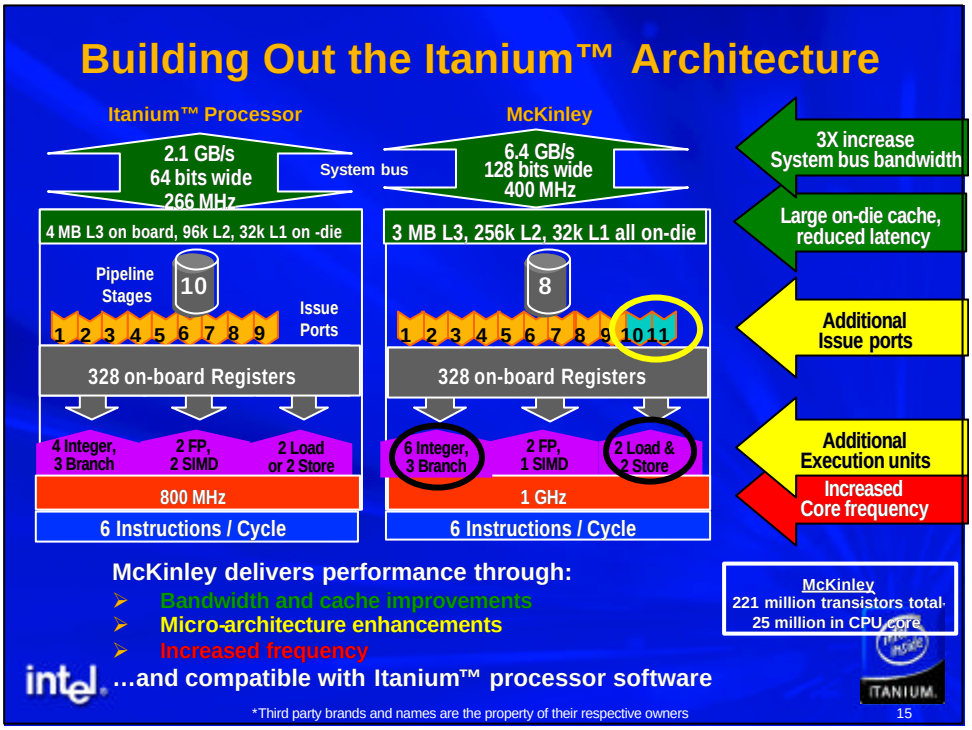
Building Out the Itanium™ Architecture
Itanium™ Processor
McKinley
2.1 GB/s
64 bits wide
266 MHz
System bus
6.4 GB/s
128 bits wide
400 MHz
3X increase
System bus bandwidth
Large on-die cache,
reduced latency
4 MB L3 on board, 96k L2, 32k L1 on -die
3 MB L3, 256k L2, 32k L1 all on-die
Pipeline
Stages
10
Issue
Ports
1 2 3 4 5 6 7 8 9
8
1 2 3 4 5 6 7 8 9 10 11
Additional
Issue ports
328 on-board Registers
328 on-board Registers
4 Integer,
3 Branch
2 FP,
2 SIMD
2 Load
or 2 Store
6 Integer,
3 Branch
2 FP,
1 SIMD
2 Load &
2 Store
Additional
Execution units
Increased
Core frequency
800 MHz
1 GHz
6 Instructions / Cycle
6 Instructions / Cycle
McKinley delivers performance through:
Bandwidth and cache improvements
Micro-architecture enhancements
Increased frequency
...and compatible with Itanium™ processor software
McKinley
221 million transistors total
25 million in CPU core
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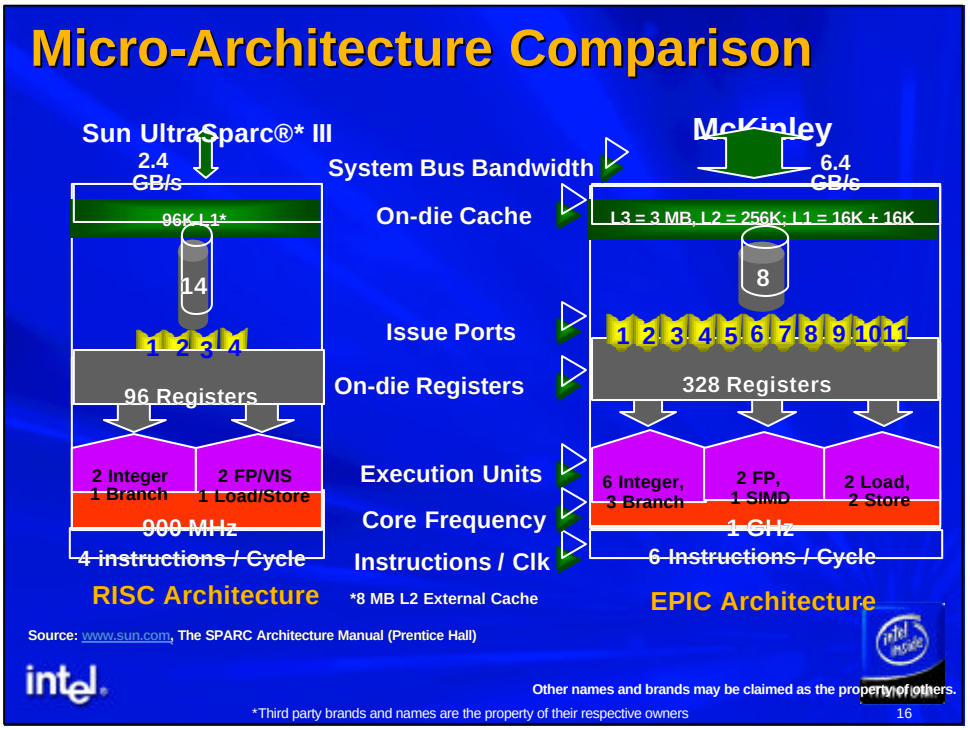
Micro-Architecture Comparison
Sun UltraSparc®* III
2.4
GB/s
System Bus Bandwidth
McKinley
6.4
GB/s
96K L1*
On-die Cache
L3 = 3 MB, L2 = 256K; L1 = 16K + 16K
14
8
1 2 3 4
Issue Ports
1 2 3 4 5 6 7 8 9 10 11
96 Registers
On-die Registers
328 Registers
2 Integer
1 Branch
2 FP/VIS
1 Load/Store
Execution Units
6 Integer,
3 Branch
2 FP,
1 SIMD
2 Load,
2 Store
900 MHz
Core Frequency
1 GHz
4 instructions / Cycle
Instructions / Clk
6 Instructions / Cycle
RISC Architecture
*8 MB L2 External Cache
EPIC Architecture
Source: www.sun.com, The SPARC Architecture Manual (Prentice Hall)
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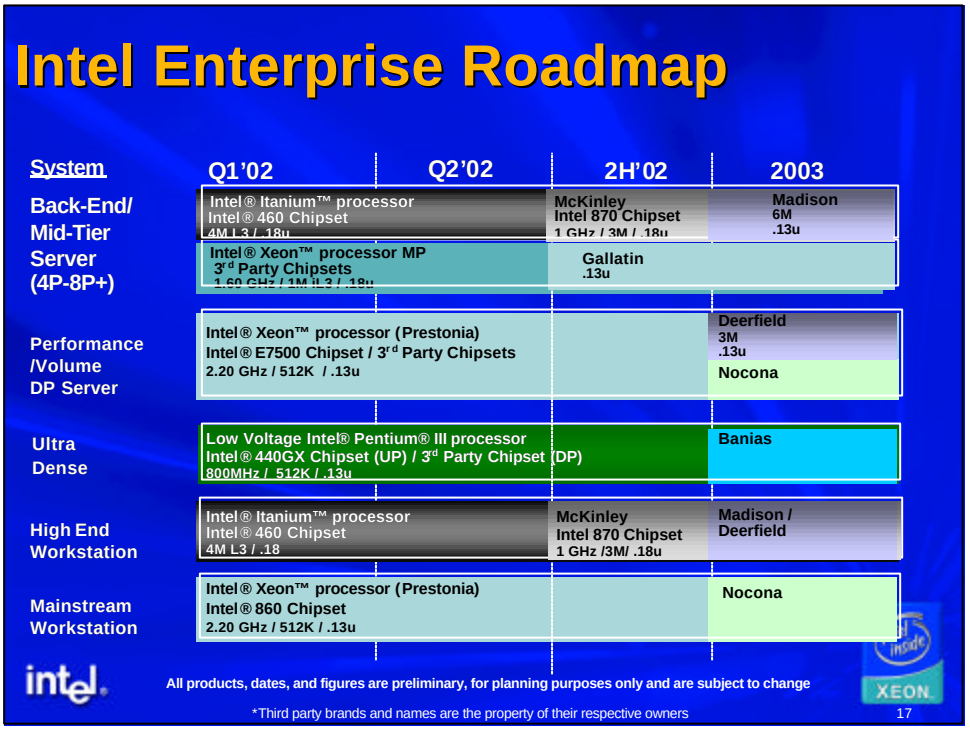
Intel Enterprise Roadmap
System
Q1'02
Q2'02
2H'02
2003
Back-End/ Mid-Tier Server (4P-8P+)
Intel® Itanium™ processor
Intel® 460 Chipset
4M L3 / .18u
McKinley
Intel 870 Chipset
1 GHz / 3M / .18u
Madison
6M
.13u
Intel® Xeon™ processor MP
3rd Party Chipsets
Gallatin
.13u
Performance /Volume DP Server
Intel® Xeon™ processor (Prestonia)
Intel® E7500 Chipset / 3rd Party Chipsets
2.20 GHz / 512K / .13u
Deerfield
3M
.13u
Nocona
Ultra Dense
Low Voltage Intel® Pentium® III processor
Intel® 440GX Chipset (UP) / 3rd Party Chipset (DP)
800MHz / 512K / .13u
Banias
High End Workstation
Intel® Itanium™ processor
Intel® 460 Chipset
4M L3 / .18
McKinley
Intel 870 Chipset
1 GHz /3M/ .18u
Madison / Deerfield
Mainstream Workstation
Intel® Xeon™ processor (Prestonia)
Intel® 860 Chipset
2.20 GHz / 512K / .13u
Nocona
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Interconnect Technology
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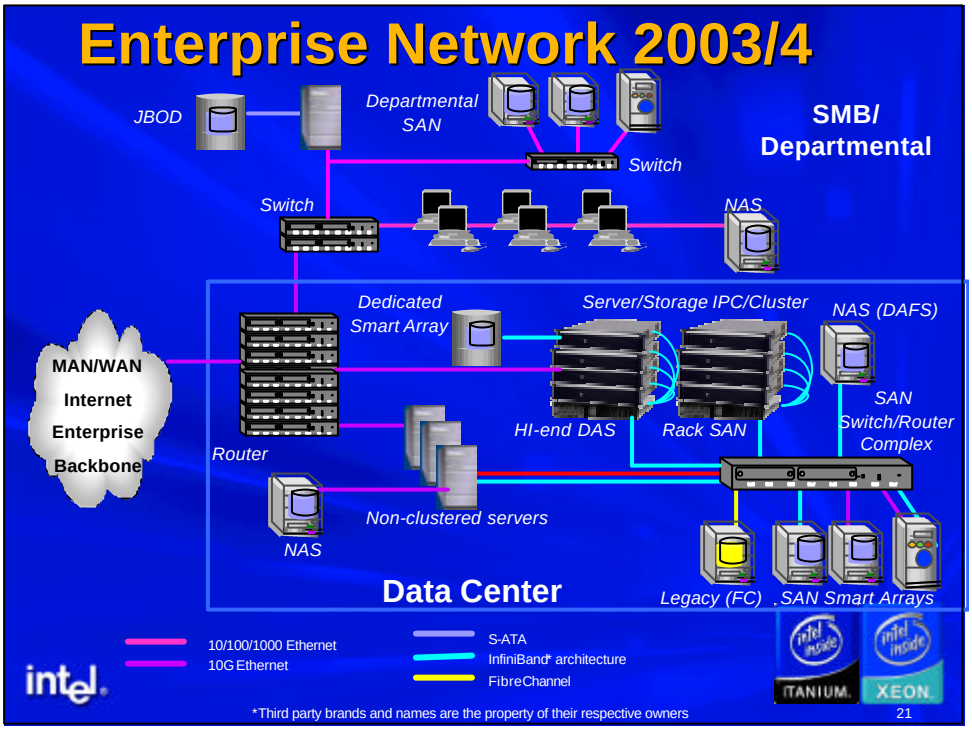
Interconnect Summary

Evolving Interconnects

		InfiniBand*	Ethernet	3GIO*
Interconnect	Chip to Chip			✓
	Blade to Blade	✓	✓	✓
	Box to Box	✓	✓	
	Site to Site		✓	
Within Data Center	High Performance (RDMA)	✓		
	IPC/Clustering	✓		
	Networking	✓	✓	
	SAN/Storage	✓	✓	
	Shared I/O	✓	✓	
	Protocols	Memory, Message SRP, DAFS, RNDIS, IPoIB, Raw, VI, SDP	TCP/IP	Memory, PCI transparent


Enterprise Network 2003/4
JBOD
Departmental SAN
SMB/ Departmental
Switch
Switch
NAS
Dedicated Smart Array
Server/Storage IPC/Cluster
NAS (DAFS)
MAN/WAN
Internet
Enterprise
Backbone
HI-end DAS
Rack SAN
SAN Switch/Router Complex
Router
Non-clustered servers
NAS
Data Center
Legacy (FC) . SAN Smart Arrays
10/100/1000 Ethernet
10G Ethernet
S-ATA
InfiniBand* architecture
FibreChannel
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Thank You