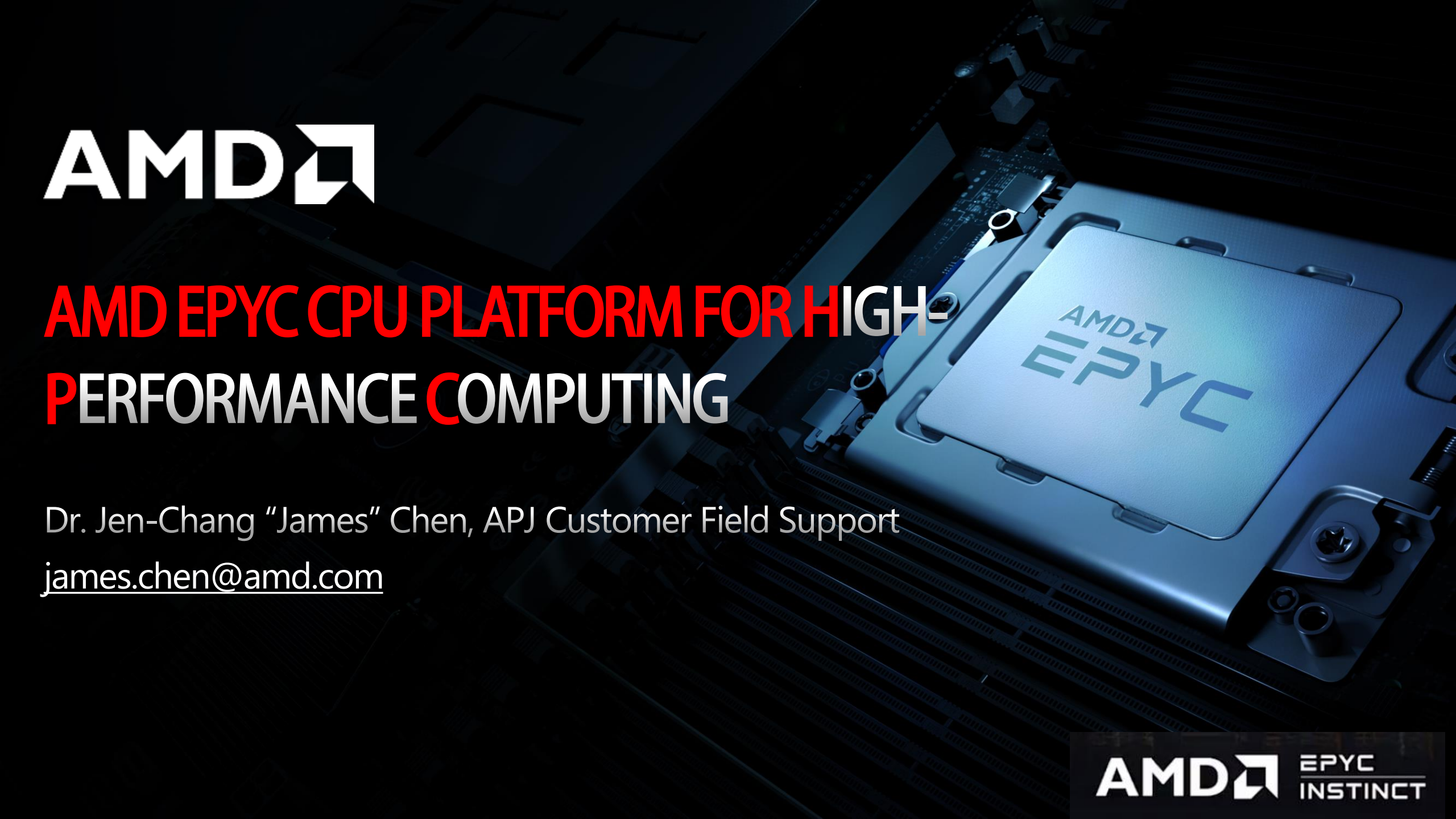


AMD EPYC CPU PLATFORM FOR HIGH-PERFORMANCE COMPUTING

Dr. Jen-Chang "James" Chen, APJ Customer Field Support

james.chen@amd.com

AMD EPYC INSTINCT

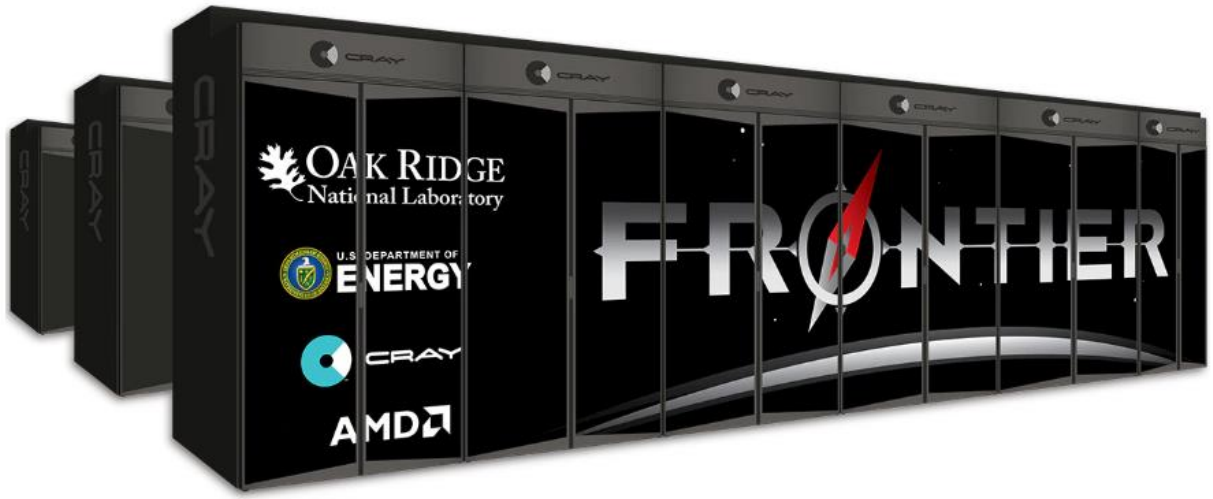
AGENDA

- Key HPC wins
- Features of AMD EPYC CPU
- Hardware architecture and software ecosystem
- Performance tuning tips
- Resources for users and developers

AMD EPYC™ HIGH PERFORMANCE COMPUTING SUCCESSES

EXA-SCALE MACHINES IN THE US

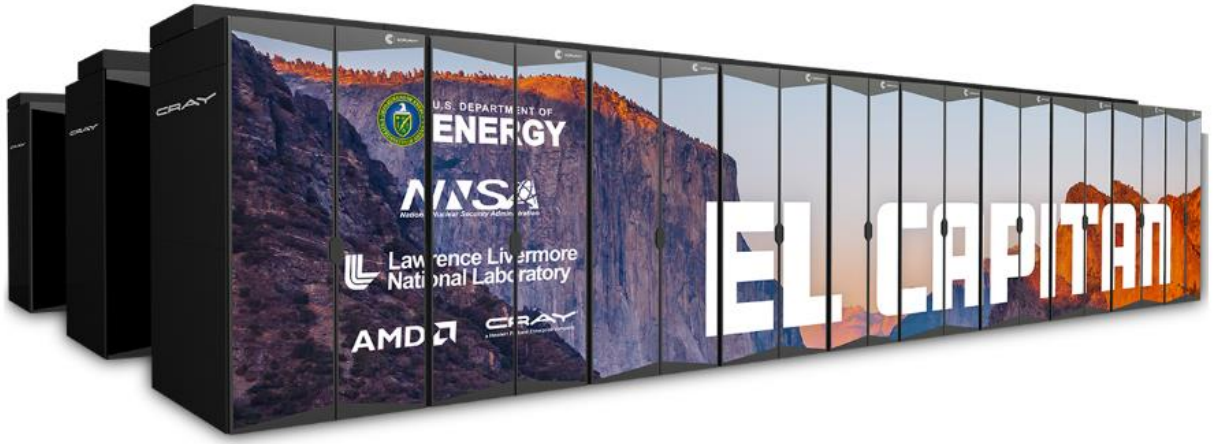
AMD Powered Exascale Supercomputers



Frontier

1.5 exaflops (ORNL in 2021)

AMD EPYC™ CPUs + HBM-enabled Radeon Instinct™ GPUs



El Capitan

2.0 exaflops (LLNL in 2023)

AMD EPYC™ CPUs + HBM-enabled Radeon Instinct™ GPUs

Reference: https://www.amd.com/en/products/exascale-era

AMD

FRONTIER SPEC SHEET

https://www.olcf.ornl.gov/wp-content/uploads/2019/05/frontier_specsheet_v4.pdf

FRONTIER Spec Sheet

The Frontier system will be composed of more than 100 Cray Shasta cabinets with high density compute blades powered by HPC and AI- optimized AMD EPYC™ processors and Radeon Instinct™ GPU accelerators purpose-built for the needs of exascale computing. The new accelerator-centric compute blades will support a 4:1 GPU to CPU ratio with high speed AMD Infinity Fabric™ links and coherent memory between them within the node. Each node will have one Slingshot interconnect network port for every GPU with streamlined communication between the GPUs and network to enable optimal performance for high-performance computing and AI workloads at exascale.

To make this performance seamless to consume by developers, ORNL and Cray will partner with AMD to co-design and develop enhanced GPU programming tools designed for performance, productivity and portability, which will tightly integrate with the existing AMD ROCm open compute platform. In addition, Frontier will support many of the same compilers, programming models, and tools that have been available to OLCF users on both the Titan and Summit supercomputers. In fact, Summit is a premier development platform for Frontier.

EPCC ARCHER2 AND HLRS HAWK

- University of Edinburgh's supercomputing center (EPCC)
- 28PF, EPYC 7H12
- General-purpose machine for R&D in the UK

- High-Performance Computing Center Stuttgart (HLRS)
- 26PF, EPYC 7742
- General-purpose machine for R&D and industry.

References

https://www.nextplatform.com/2019/10/18/amd-cpus-will-power-uks-next-generation-archer2-supercomputer/

https://www.hlrs.de/systems/hpe-apollo-hawk/

AMD

LUMI AND PAWSEY SC

- Lumi in CSC's data center in Kajaani, Finland (2021)
- 552PF **AMD EPYC™ CPUs +** HBM-enabled Radeon Instinct™

- Phase 1 in Q3 2021; Full system in Q2 2022

References

https://www.lumi-supercomputer.eu/lumi-one-of-the-worlds-mightiest-supercomputers/

https://pawsey.org.au/powering-the-next-generation-of-australian-research-with-hpe/

INDUSTRY'S FIRST GPU TO BREAK 10 TF (FP64) BARRIER

2000

ASCI White, #1 Supercomputer

6 Megawatts, 212K Pounds (106 Tons), 12.3 Teraflops Peak

2020

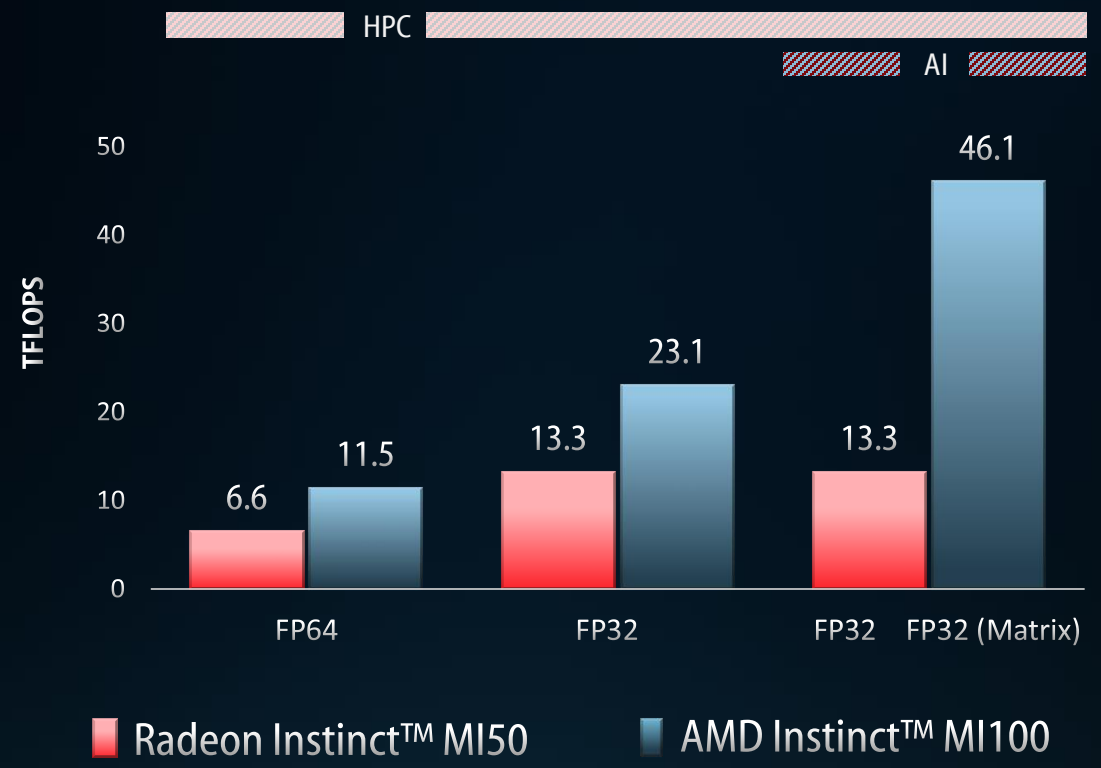
AMD Instinct™ MI100 GPU

300 Watts, 2.56 Pounds (1.16Kg), 11.5 Teraflops Peak

SEE ENDNOTES MI100-03

AMD INSTINCT™ MI100: GENERATIONAL GAIN FOR HPC & AI

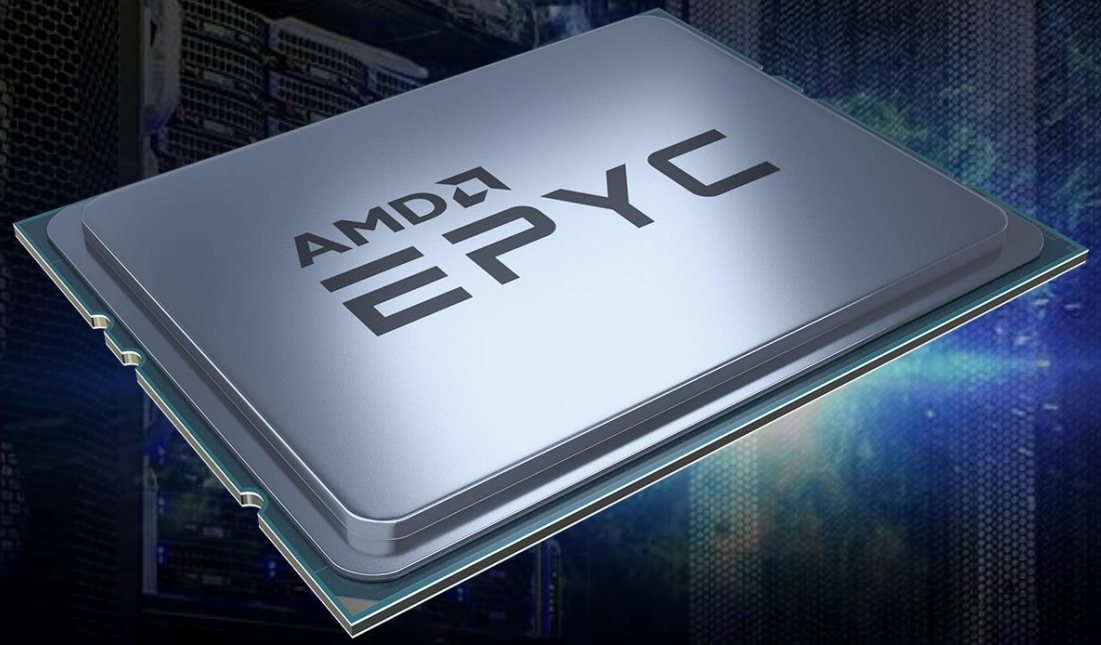
SETTING NEW BAR FOR PERFORMANCE



SEE ENDNOTES, MI100-04, MI100-05, MI100-16

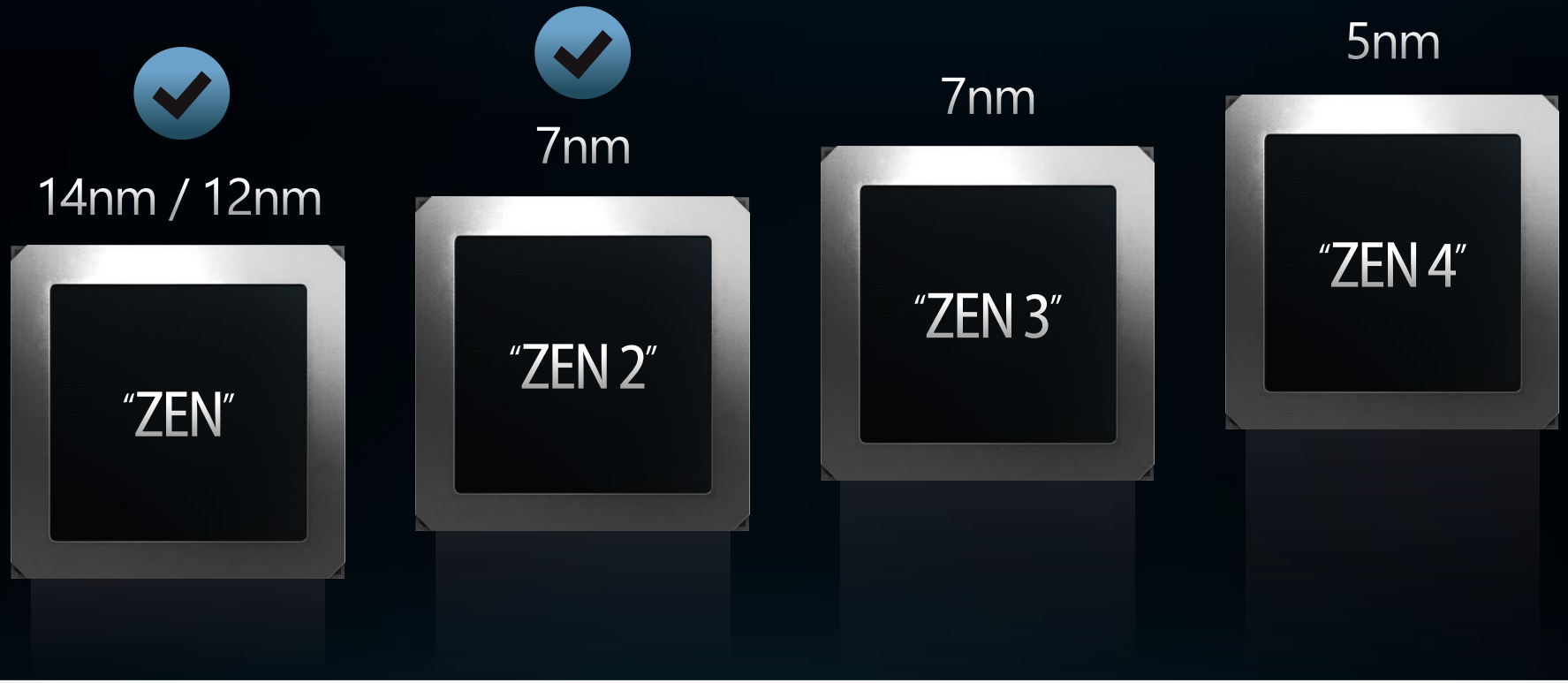
AMD

"ZEN" CORE EVOLUTION & ARCHITECTURE



CPU ROADMAP

SUSTAINED HIGH-PERFORMANCE LEADERSHIP



Roadmap Subject to Change

AMD

LEADING EDGE 7NM PROCESS TECHNOLOGY

Major Node, Significant Investment

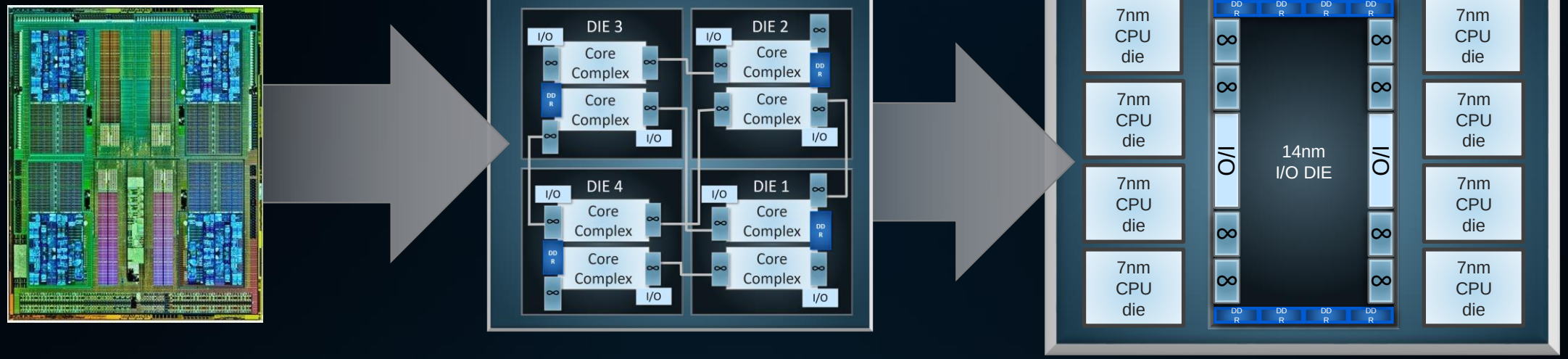
Faster, Smaller, Lower-Power Transistors

2X Density

Half Power at Same Performance

See Endnote EPYC-07

MULTICHIP ARCHITECTURE REVOLUTION

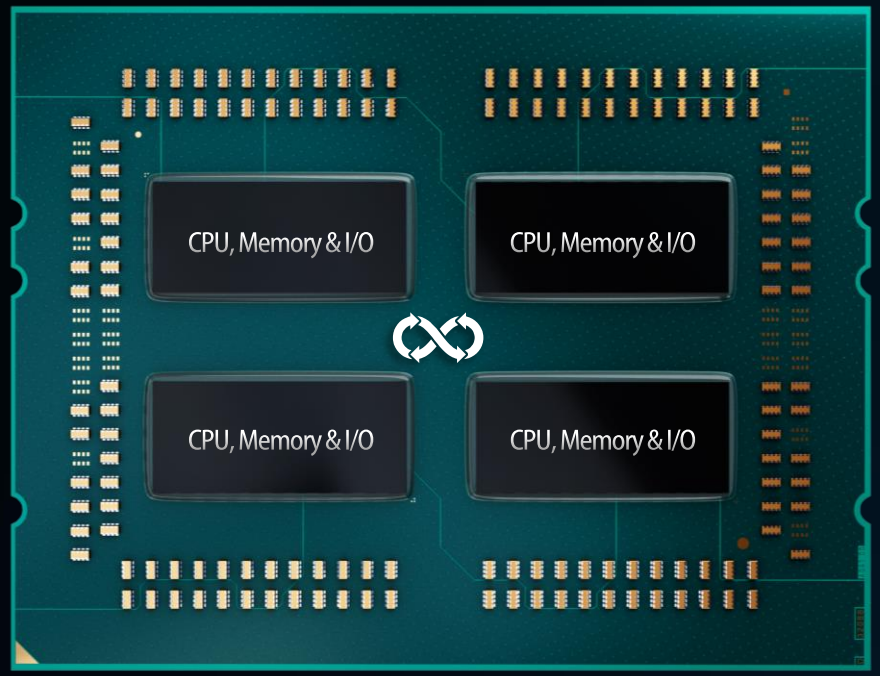


Monolithic die

Multi-die Multi-Chip Module

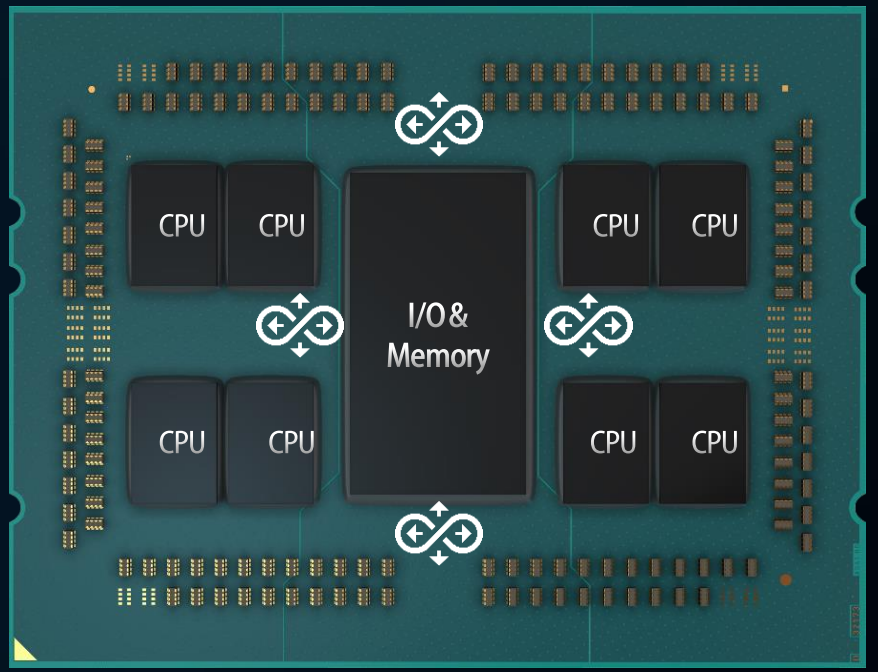
Chiplet

1st Gen AMD EPYC



Four SOCs Interconnected
via 1st Gen AMD Infinity Architecture

2nd Gen AMD EPYC



Eight 7nm Chiplet CPUs and One 14nm Chiplet I/O
Interconnected via 2nd Gen AMD Infinity Architecture

Each IP in its Optimal Process Technology | Distributed Control | I/O Die and CPU Die Optimizes Latency and Power | Flexible and More Unified Memory Architecture

AMD

AMD EPYC™ 7002 SERIES PROCESSORS AT A GLANCE

- 7001 SERIES FOUNDATION WITH INCREASED PERFORMANCE, CAPABILITIES, AND ADVANCED SECURITY

COMPUTE

Up to 2X AMD "Zen" x86 cores
(up to 64 cores/128 threads)

Up to 4X shared L3 cache (256MB)
Up to 2X L3 cache per core
(16MB per 4 cores)

Reduced System Diameter
(NUMA domain)

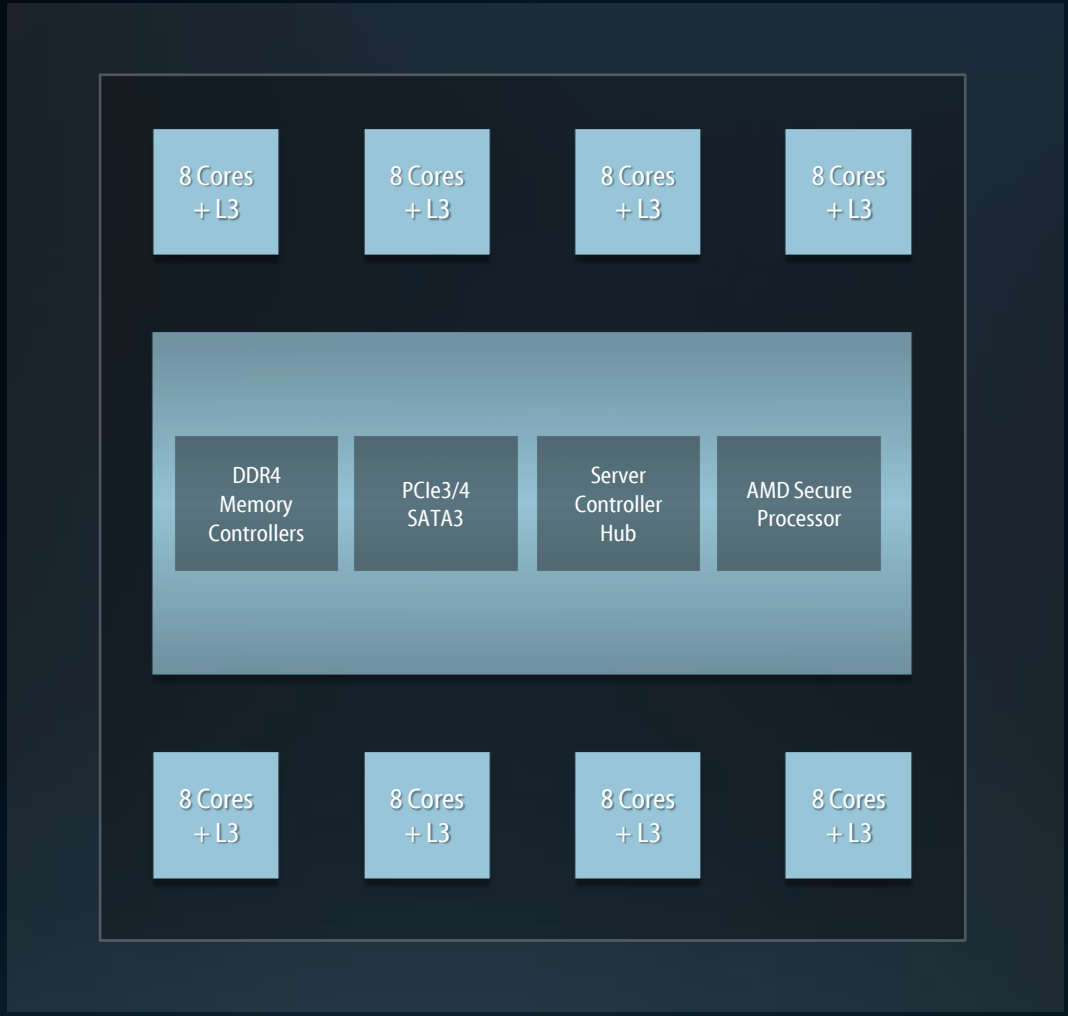
TDP range: 120W-280W*

MEMORY

8 channel DDR4 with ECC
up to 3200 MHz*

RDIMM, LRDIMM, 3DS, NVDIMM

2 DIMMs/channel capacity of 4TB/socket



PERFORMANCE

~4x Peak TFLOPS/Socket
~2X increased perf/socket

INTEGRATED I/O – NO CHIPSET

128 lanes PCIe® 3 & 4*
- Used for PCIe, SATA, and Coherent Interconnect
- Up to 32 SATA or NVMe devices

SECURITY

Dedicated Security Subsystem

Hardware Root-of-Trust

Additional Security Features

SME, SEV, SEV-ES

* A MOTHERBOARD DESIGNED FOR 2ND GEN EPYC PROCESSORS IS REQUIRED TO ENABLE ALL FUNCTIONALITY. SEE ENDNOTE ROM-06

SEE ENDNOTES ROM-04, 07, 342

AMD

HOW DO WE CALCULATE THE THEORETICAL HPL VALUE?

AMD EPYC™ 7742

Specifications

# of CPU Cores: 64	**# of Threads:** 128	**Base Clock:** 2.25GHz
Max Boost Clock: Up to 3.4GHz	**Total L3 Cache:** 256MB	**Package:** SP3
Socket Count: 1P/2P	**PCI Express® Version:** PCIe 4.0 x128	**Default TDP / TDP:** 225W

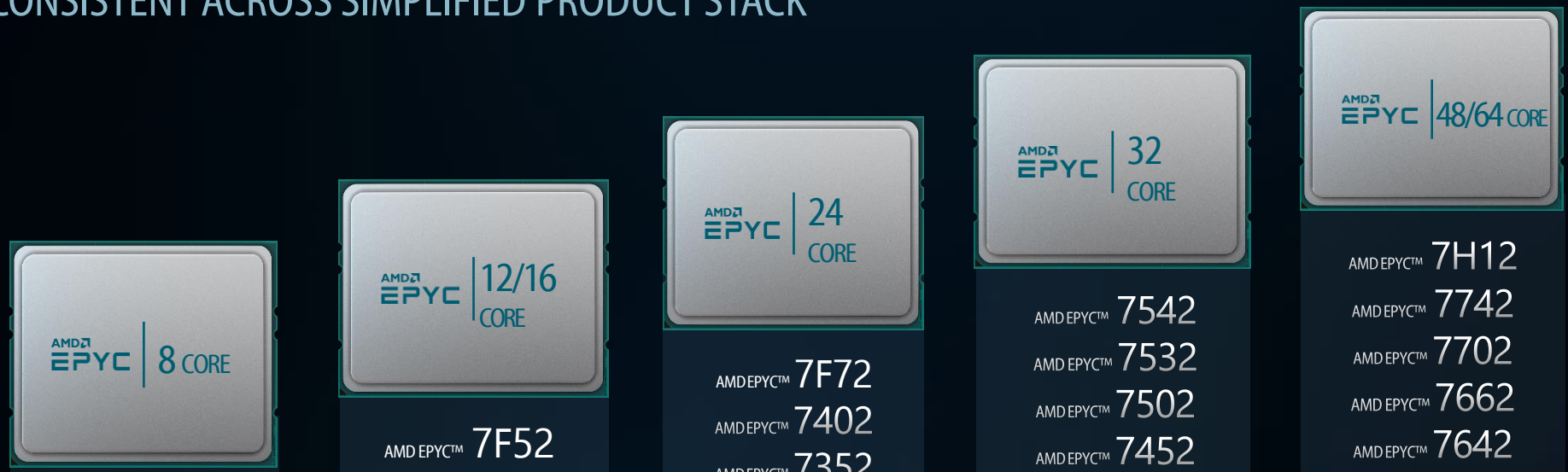
- Dual-socket AMD 7742 CPUs per node
- Rpeak = 2 x # of CORES x Base Freq x 16 (AVX2 DP FLOPS)
- Rpeak = 2 x 64 x 2.25 GHz x 16 = 4,608 GFLOPS
- Rmax = 4,000 GFLOPS (HPL 2.3 output)

- Is HPL a good metric?

Reference: https://www.amd.com/en/products/cpu/amd-epyc-7742#product-specs

AMD EPYC™ PROCESSORS DELIVER THE POWER OF SIMPLICITY

ADVANCED FEATURES CONSISTENT ACROSS SIMPLIFIED PRODUCT STACK



	8 CORE	12/16 CORE	24 CORE	32 CORE	48/64 CORE
SINGLE- & DUAL-SOCKET	AMD EPYC™ 7F32 AMD EPYC™ 7262 AMD EPYC™ 7252	AMD EPYC™ 7F52 AMD EPYC™ 7302 AMD EPYC™ 7282 AMD EPYC™ 7272	AMD EPYC™ 7F72 AMD EPYC™ 7402 AMD EPYC™ 7352	AMD EPYC™ 7542 AMD EPYC™ 7532 AMD EPYC™ 7502 AMD EPYC™ 7452	AMD EPYC™ 7H12 AMD EPYC™ 7742 AMD EPYC™ 7702 AMD EPYC™ 7662 AMD EPYC™ 7642 AMD EPYC™ 7552
SINGLE-SOCKET	AMD EPYC™ 7232P	AMD EPYC™ 7302P	AMD EPYC™ 7402P	AMD EPYC™ 7502P	AMD EPYC™ 7702P

All-in feature set includes:
8 Channels of DDR4-3200*
4TB memory capacity
128 lanes PCIe® 4*
SMT & Turbo boost
18G Infinity Fabric™
Secure Memory Encryption
Secure Encrypted Virtualization

* A MOTHERBOARD DESIGNED FOR 2ND GEN EPYC PROCESSORS IS REQUIRED TO ENABLE ALL FUNCTIONALITY. SEE ENDNOTE ROM-06

AMD

WORKLOAD AFFINITY

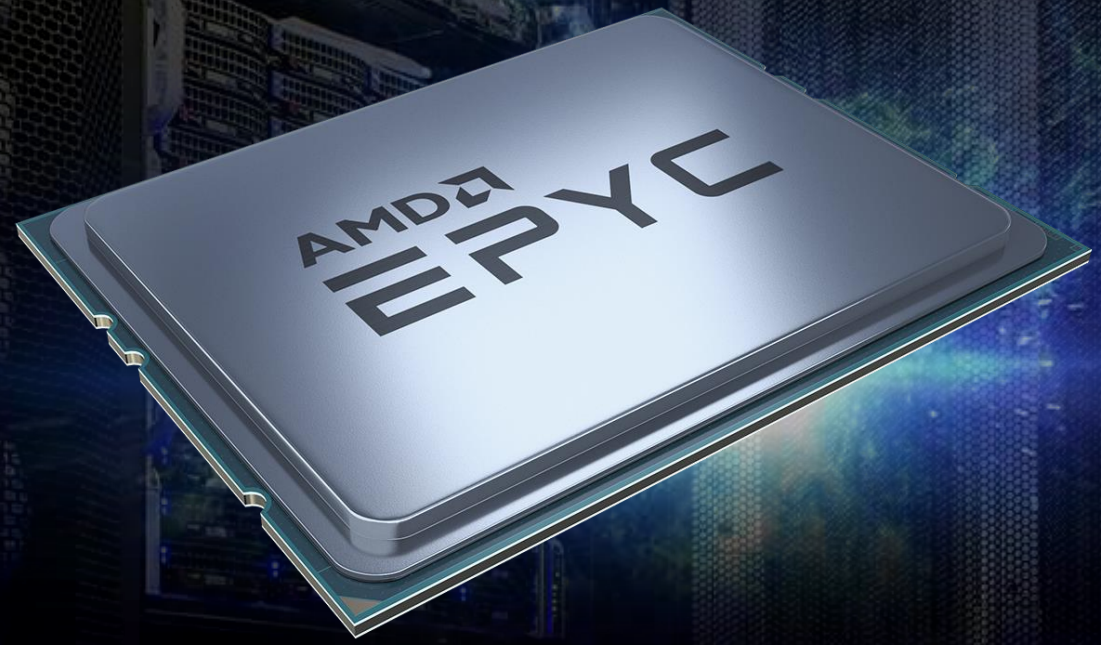
- Core-count
- L3 cache
- 8 memory channels per CPU
- PCIe gen 4

Model	Cores	Socketss	Workload Affinity
7H12	64	2P/1P	Specialized CAE/CFD/FEA
7742	64	2P/1P	High capacity data mgmt (NR/RDBMS), analytics, VM density, HPC parallel, CAE/CFD/FEA, ERM/SCM/CRM apps
7702	64	2P/1P	
7702P		1P	Value data mgmt (NR/RDBMS), VM density, ERM/SCM/CRM apps, security
7662	64	2P/1P	High capacity data mgmt (NR/RDBMS), analytics, VM density, CAE/CFD/FEA, ERM/SCM/CRM apps, VDI, app dev/test
7642	48	2P/1P	
7552	48	2P/1P	
7542	32	2P/1P	Medium capacity data mgmt (NR/RDBMS), analytics, VM density, CAE/CFD/FEA, ERM/SCM/CRM apps, VDI, media streaming
7532	32	2P/1P	
7502	32	2P/1P	
7502P		1P	Value data mgmt (NR/RDBMS), VM density, ERM/SCM/CRM apps, VDI
7452	32	2P/1P	General purpose, content mgmt, app dev/test
7F72	24	2P/1P	High performance VM density, VDI, HCI, EDA, per-core CAE/CFD/FEA
7402	24	2P/1P	General purpose, per core CAE/CFD/FEA GPU/FPGA accelerated, SW-defined storage
7402P		1P	Value general purpose, SW-defined storage
7352	24	2P/1P	Web serving, networking/NFV, ERM/SCM/CRM apps
7F52	16	2P/1P	EDA, per core CAE/CFD/FEA, high-speed data mgmt (NR/RDBMS)
7302	16	2P/1P	Per core CAE/CFD/FEA, EDA, media streaming
7302P		1P	Value per core CAE/CFD/FEA, EDA, media streaming
7282	16	2P/1P	Cost-optimized general purpose, SW-defined storage
7272	12	2P/1P	Cost-optimized general purpose, content mgmt
7F32	8	2P/1P	licensed per core data mgmt (RDBMS), departmental CAE/CFD/FEA, EDA, FSI risk analysis
7262	8	2P/1P	Cost-optimized, licensed per core data mgmt (RDBMS), optimal CAE/CFD/FEA, EDA, collaborative
7252	8	2P/1P	
7232P	8	1P	Value, cost-optimized per core license

NOTE: This guide is designed to provide a high-level workload assessment based on AMD engineering estimates. Performance varies depending on system configuration.

AMD

EPYC™ 7002 SERIES PROCESSOR PERFORMANCE



NEW LEADER, NEW RULES

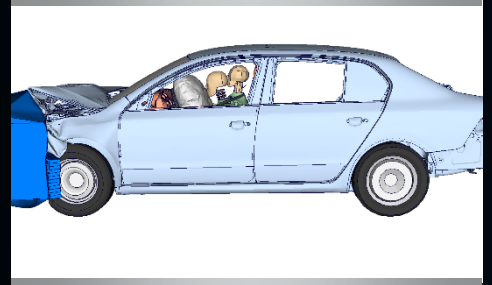
170+ WORLD RECORDS AND COUNTING

BIG DATA	31	Big Data and Analytics**
CLOUD	10	Cloud and Virtualization
HPC	25	High-Performance Computing Apps
	12	Floating Point Performance
	12	Floating Point Energy Efficiency
SDI/ENTERPRISE	10	Integer Performance
	44	Java®-based Performance
	8	DB/ERP Business Applications
	21	Energy Efficiency

** INCLUDES TIES WHICH ARE NOT COUNTED IN THE AMD WORLD RECORDS TOTAL NUMBER

World records as of June 9, 2020. See AMD.com/worldrecords for details

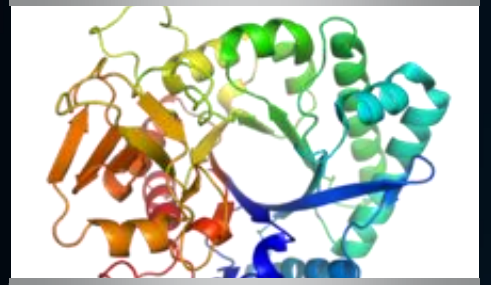
LEADERSHIP PERFORMANCE
WITH REAL WORLD HPC RESULTS



ENGINEERING SIMULATIONS

esi get it right®

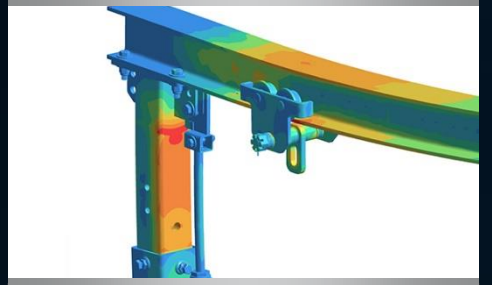
UP TO 58%
HIGHER PERFORMANCE



LIFE SCIENCES

GROMACS

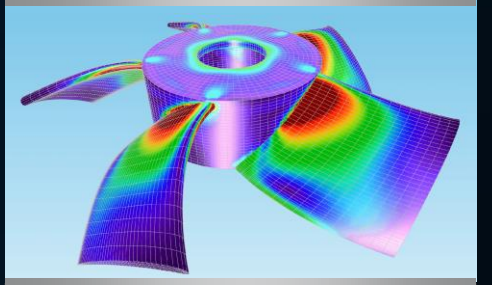
UP TO 60%
HIGHER PERFORMANCE



STRUCTURAL ANALYSIS

Altair

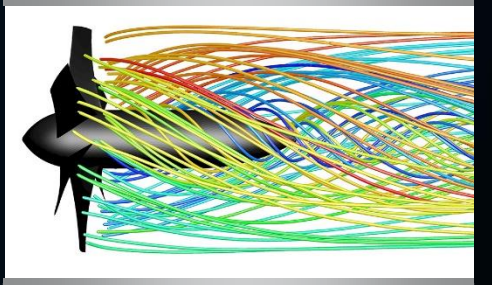
UP TO 72%
HIGHER PERFORMANCE



FINITE ELEMENT ANALYSIS

LSTC Livermore Software Technology Corp.

UP TO 79%
HIGHER PERFORMANCE



FLUID DYNAMICS

ANSYS®

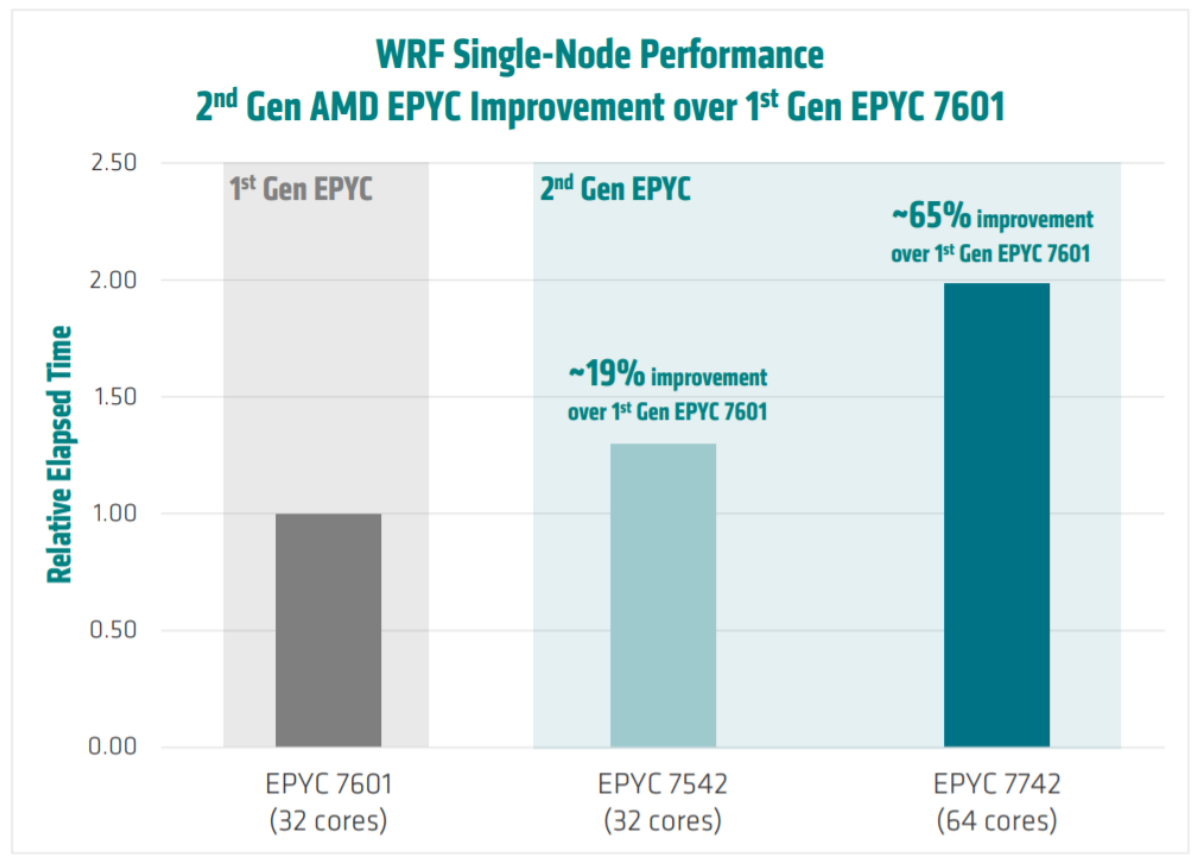
UP TO 95%
HIGHER PERFORMANCE

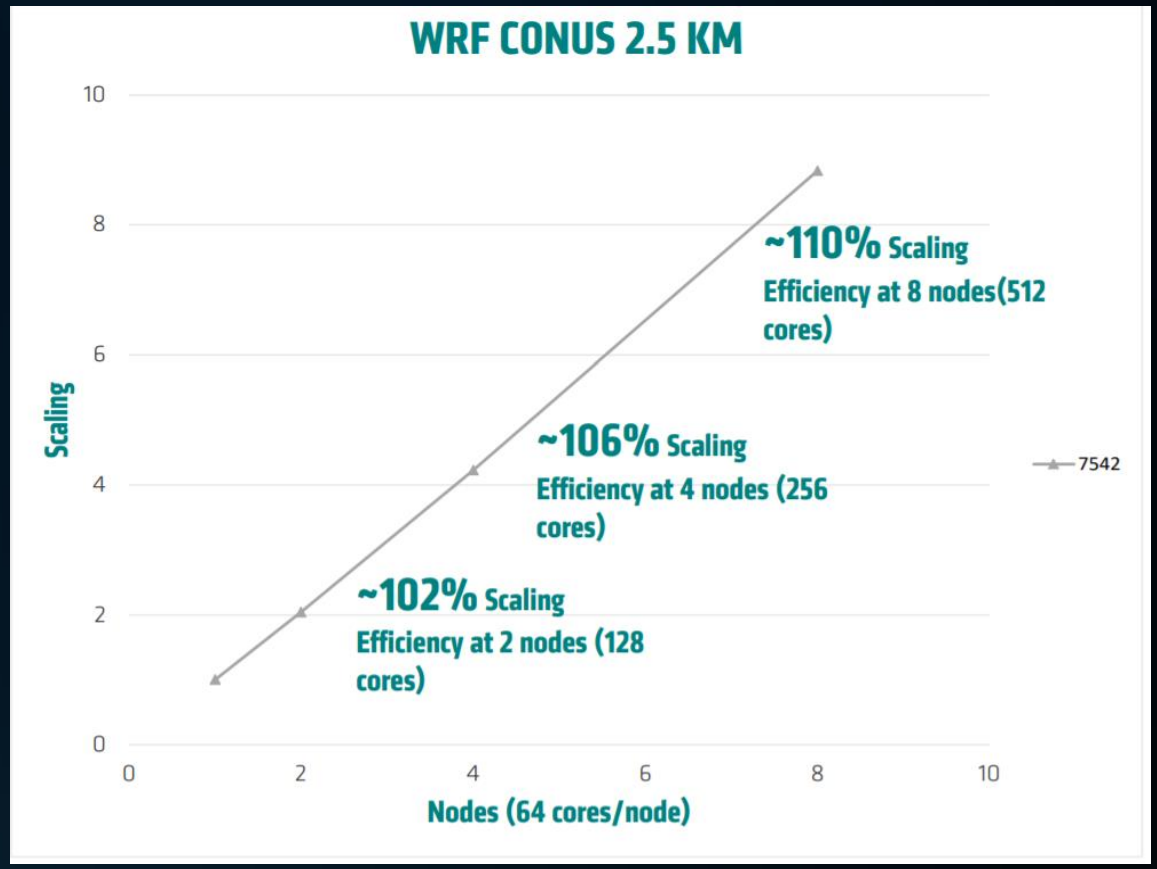
EPYC™ 7742 versus Xeon® 8280. SEE ENDNOTES ROM-63, ROM-113, ROM-56, ROM-49, ROM-42

AMD

WRF (WEATHER RESEARCH)

Exceptional scaling of this magnitude can be attributed to **cache effects** fitting more of the model into the processor cache.

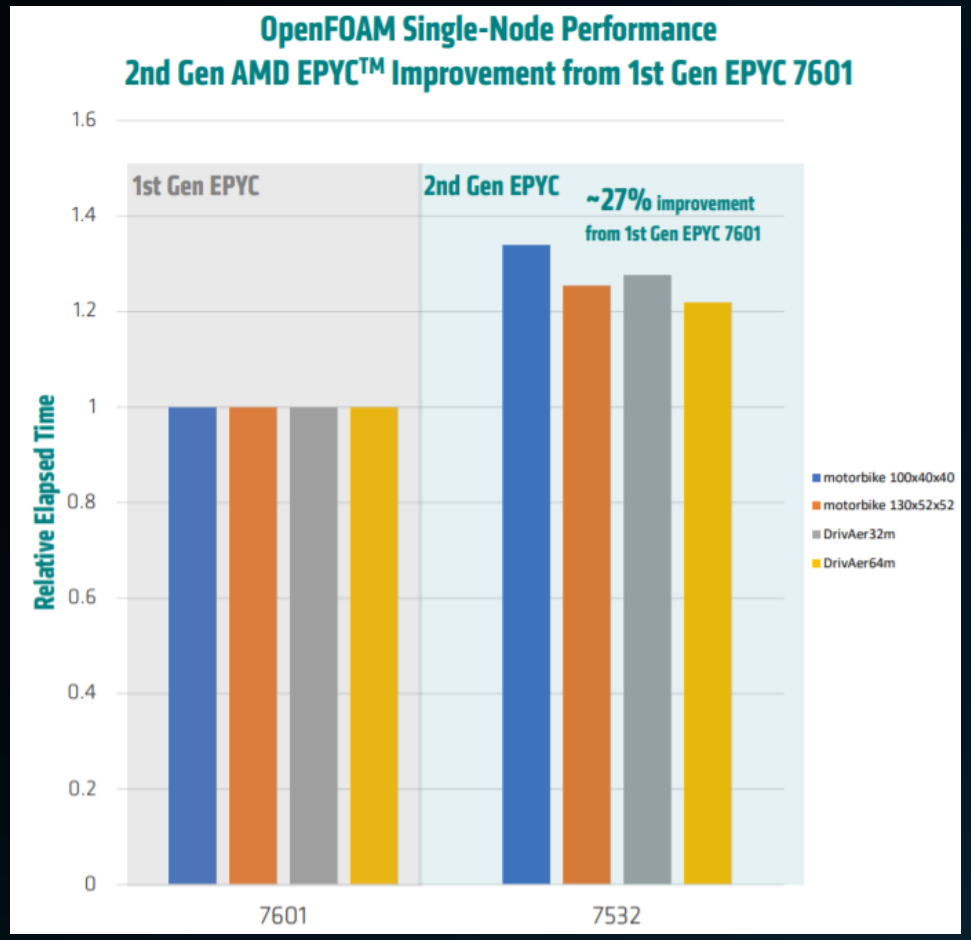


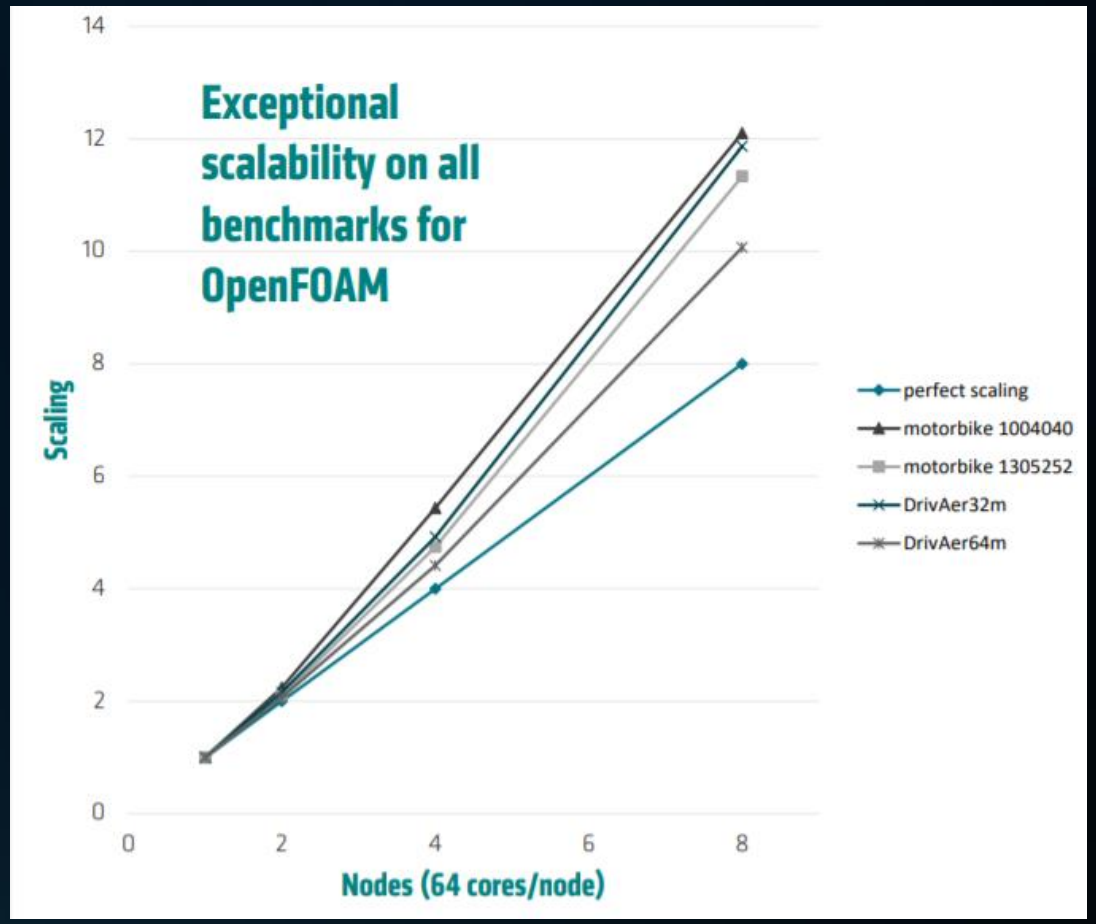


Reference: https://www.amd.com/system/files/documents/EPYC-7002-Weather-Modeling-with-WRF.pdf

OPENFOAM (CFD)

The highest super-linear scalability for multi-node calculation is due to the benefit of **cache memory advantage**.

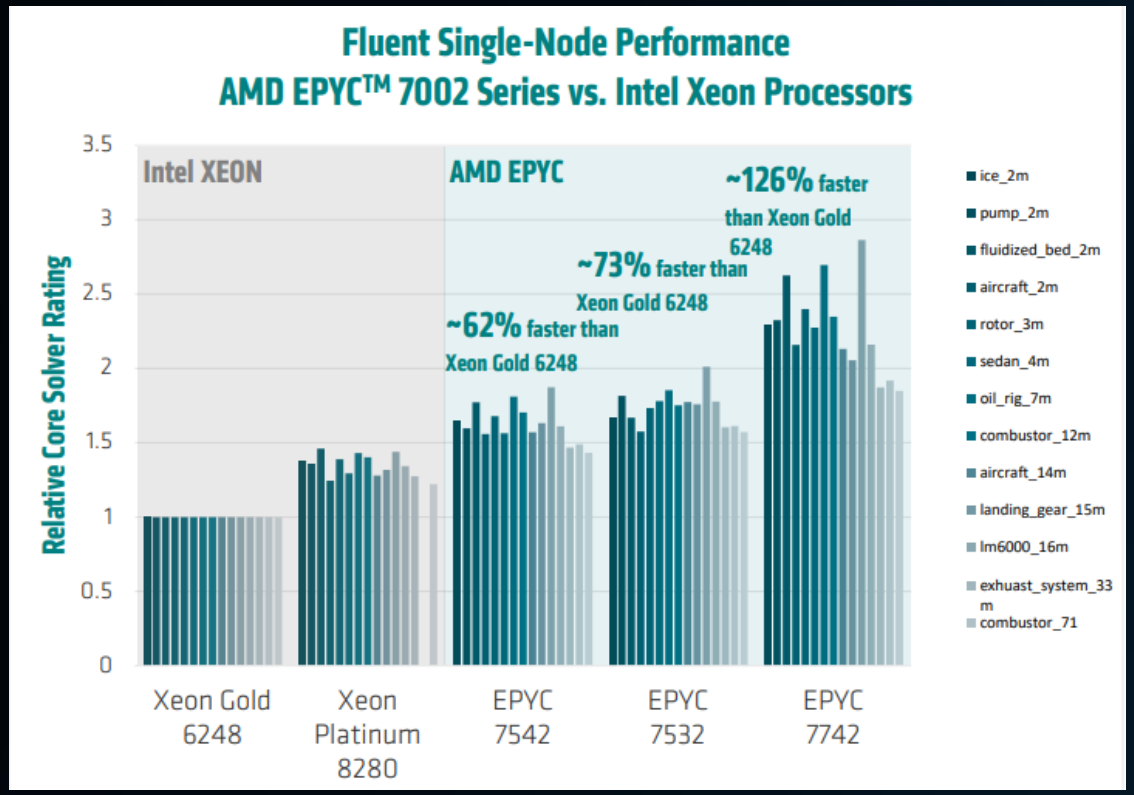


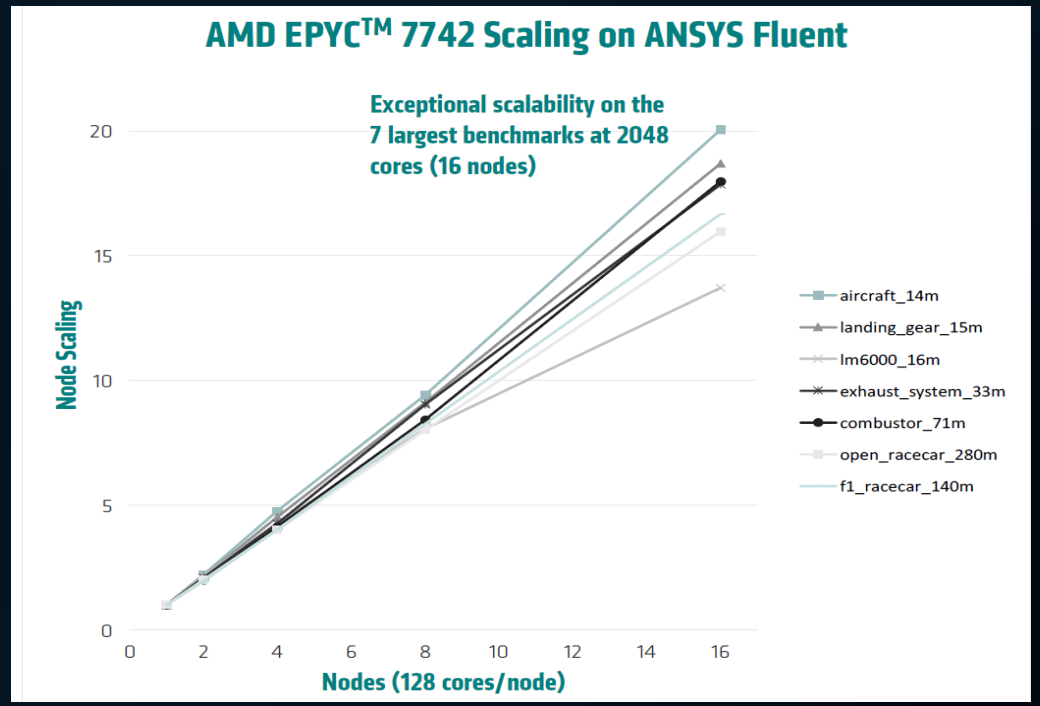


Reference: https://www.amd.com/system/files/documents/AMD-EPYC-7002-OpenFOAM.pdf

AMD

ANSYS FLUENT (CFD)





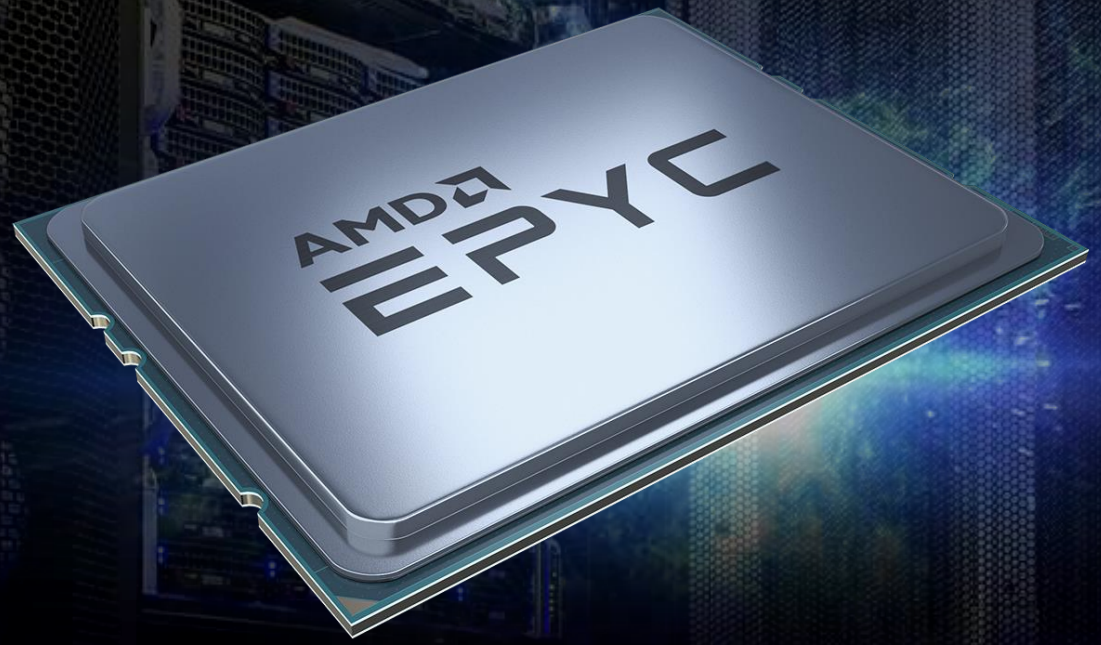
Intel-based Compute Nodes		
CPUs	2 x Intel Xeon Gold 6248	2 x Intel Xeon Platinum 8280
Cores	20 cores per socket (40 per node)	28 cores per socket (56 per node)
Memory	768 GB (12x) Dual-Rank DDR4-2933, 1 DPC (Samsung)	384 GB (12x) Dual-Rank DDR4-2933, 1 DPC (Micron)
Storage: OS | Data	1 x 240 GB SATA | 1 x 500 GB NVMe	
Software		
OS	RHEL 7.6 (3.10.0-862.el7.x86_64)	
Configuration Options		
BIOS Setting	Default, plus: Power Management = Max Performance, Hyper-threading=Off, SNC=On, ADDDC=Off	
OS Settings	Overridden by BIOS Power Management Settings	

Tested Hardware and Software Configuration

AMD Compute Nodes			
CPUs	2 x EPYC 7742	2 x EPYC 7542	2 x EPYC 7532
Cores	64 cores per socket (128 per node)	32 cores per socket (64 per node)	32 Cores socket (64 per node)
Memory	Micron 1 TB (16x) Dual-Rank DDR4-3200, 1DPC		
Network Adapter	Mellanox ConnectX-6 HDR 200Gb/s Infiniband x16 PCIe® Gen 4		
Storage: OS | Data	1 x Micron 1100 256 GB SATA | 1 x 1 TB NVMe		
Software			
OS	RHEL 7.6 (3.10.0-862.el7.x86_64)		
Mellanox OFED Driver	MLNX_OFED_LINUX-4.5-1.0.1.0 (OFED-4.5-1.0.1)		
Network			
Switch	Mellanox 200Gb/s HDR InfiniBand Switch (MQM8790)		
Configuration Options			
BIOS Setting	NPS = NPS4, SMT = Off, Boost = On, X2APIC = On, Determinism Slider = Performance, Preferred IO=Enabled		
OS Settings	Governor=Performance, CC6 = Disabled		

Reference: https://www.amd.com/system/files/documents/AMD-EPYC-7002-AnsysFluent-Scalability-Performance.pdf

COMPILERS AND LIBRARIES



EPYC™ COMPILER AND LIBRARY SUPPORT

AOCC (AMD Optimizing C/C++ Compiler)

CPU Libraries

µProf (Performance & Power Profiling Tools)

AMD EPYC™ PROCESSOR COMPILER SUPPORT

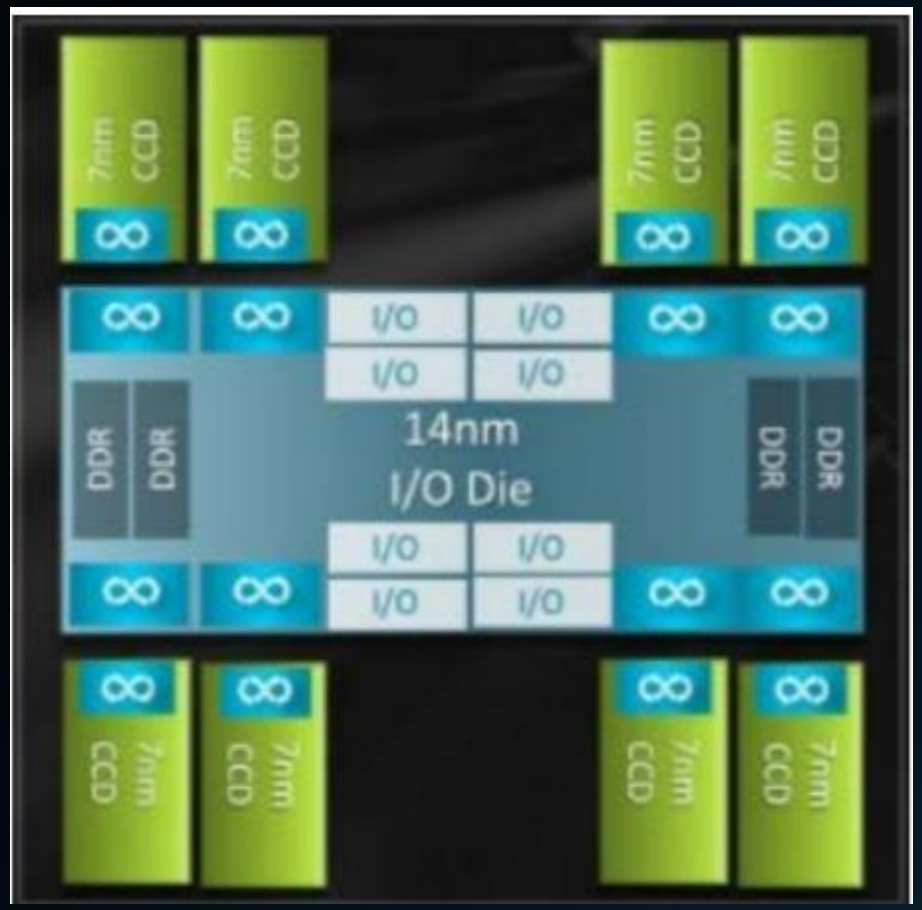
AN OPEN SOURCE STRATEGY

Performance Compilers	**AOCC**	AMD Optimizing C/C++ Compiler – Built on LLVM and Optimized for EPYC Processors
	OpenJDK / Java ORACLE	Java Compiler and Runtime - AMD contributes enablement and optimization to OpenJDK; Oracle then incorporates in their releases
Platform Compilers	LLVM	AMD is actively involved in the LLVM community and will upstream EPYC processor optimizations implemented in AOCC
	GCC	Widely used Open Source compiler - AMD upstreams processor enablement and tuning for EPYC
	Visual Studio	Widely used Windows compiler – AMD contributes processor enablement and tuning for EPYC
Ecosystem Compilers	PGI, Intel & Others	Can utilize other popular compilers on AMD platforms. https://www.aravision.com/products/pgi/pdf/pgirn.pdf https://www.amd.com/system/files/documents/compiler-options-guide-amd-epyc-7xx1-series-processors.pdf

PERFORMANCE TUNING TIPS

- Read the HPC tuning guide
  - https://developer.amd.com/wp-content/resources/56827-1-0.pdf
- Review the hardware specification (especially AMD EPYC SKU and memory)
- Tune the BIOS parameters (See Chapter 4 of the HPC tuning guide)
- Compile the program with the right flags and check the settings of math libs
  - Intel compiler: -O3 -march=core-avx2 –ip
  - GCC: -Ofast -mavx2 -mfma
  - AOCC: -Ofast -march=znver2 -mavx2
- Map the process with hardware architecture (numactl or other runtime APIs)

MAP THE WORKLOAD WITH THE CPU ARCHITECTURE



- OPENMP (1-node Dual-7742)
- export OMP_NUM_THREADS=32
- export OMP_BIND_PROC=true
- export GOMP_CPU_AFFINITY=0-127:4

- OPENMPI+OPENMP (1-node Dual-7742)
- export OMP_NUM_THREADS=4
- mpirun -np 32 --bind-to l3cache My_PROGRAM

- Reference: https://developer.amd.com/wp-content/resources/56827-1-0.pdf

USEFUL REFERENCES

- EPYC selector: https://www.amd.com/en/processors/epyc-cpu-selector
- Comparisons of AMD product specification: https://www.amd.com/en/products/specifications/
- AMD CPU resources for DEV: https://developer.amd.com/resources/epyc-resources/
- AMD AOCC (Compiler): https://developer.amd.com/amd-aocc/
- AMD AOCL (Library): https://developer.amd.com/amd-aocl/
- AMD white paper on real applications: https://www.amd.com/en/processors/server-tech-docs/
- External resources
  - https://prace-ri.eu/wp-content/uploads/Best-Practice-Guide_AMD.pdf
  - https://www.dell.com/support/article/en-sg/sln319015/amd-rome-is-it-for-real-architecture-and-initial-hpc-performance?lang=en
  - https://hpcadvisorycouncil.atlassian.net/wiki/spaces/HPCWORKS/pages/1280442391/AMD+2nd+Gen+EPYC+CPU+Tuning+Guide+for+InfiniBand+HPC

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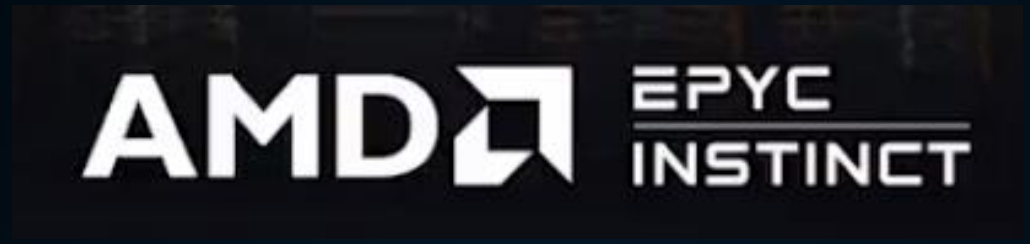

ENDNOTES

- EPYC-07 - Based on June 8, 2018 AMD internal testing of same-architecture product ported from 14 to 7 nm technology with similar implementation flow/methodology, using performance from SGEMM.
- **ROM-04** Based on standard calculation method for determining FLOPS. ROM-04
- ROM-06 - Some supported features and functionality of 2nd Gen AMD EPYC™ processors require a BIOS update from your server manufacturer when used with a motherboard designed for the 1st Gen AMD EPYC series processor. A motherboard designed for 2nd Gen EPYC processors is required to enable all available functionality.
- ROM-07 - Motherboards designed for 1st Gen EPYC processors may not be compatible with 2nd Gen AMD EPYC processors with a TDP greater than 200 watts. Contact the server manufacturer to confirm compatibility.
- ROM-342
  1-n, 2-socket 2nd Gen EPYC™ 7742 powered server (http://spec.org/cpu2017/results/res2019q4/cpu2017-20191125-20001.pdf) scoring 701 SPECrate®2017_int_base has up to 2.3x the SPECrate® 2017 Integer (Base) performance of the highest previous generation score of 304 SPECrate®2017_int_base by a 1-n, 2-socket 1st Gen EPYC™ 7601 powered server result (http://www.spec.org/cpu2017/results/res2019q2/cpu2017-20190411-11817.html) as of 1/26/20. ROM-342

- ROM-741: Best published SPECrate®2017_int_base performance as of 9/29/2020.
  AMD EPYC 2P processor scores reflect highest scoring processor at each available core level (core count is per processor):
  AMD EPYC 7742 (64C) score of 701 http://spec.org/cpu2017/results/res2019q4/cpu2017-20191125-20001.pdf
  AMD EPYC 7642 (48C) score of 586 http://spec.org/cpu2017/results/res2020q3/cpu2017-20200622-23009.html
  AMD EPYC 7542 (32C) score of 437 http://spec.org/cpu2017/results/res2020q3/cpu2017-20200706-23309.html
  AMD EPYC 7302 (16C) score of 246 http://spec.org/cpu2017/results/res2020q1/cpu2017-20191220-20441.pdf
  AMD EPYC 7262 (8C) score of 135 http://spec.org/cpu2017/results/res2020q2/cpu2017-20200608-22777.html

  Intel® Xeon® Scalable 2P processors scores using the highest competitive part in the Bronze, Silver and Gold metal classes:
  Intel Xeon Gold 6258R (28C) score of 397 http://spec.org/cpu2017/results/res2020q3/cpu2017-20200915-23981.html
  Intel Xeon Gold 5220R (24C) score of 319 http://spec.org/cpu2017/results/res2020q3/cpu2017-20200608-22594.html
  Intel Xeon Silver 4216 (16C) score of 193 http://spec.org/cpu2017/results/res2020q3/cpu2017-20200804-23653.html
  Intel Xeon Bronze 3206R (8C) score of 60.1 http://spec.org/cpu2017/results/res2020q2/cpu2017-20200609-22881.html
  SPEC®, SPECrate® and SPEC CPU® are registered trademarks of the Standard Performance Evaluation Corporation. See w ww.spec.org for more information ROM-741

ENDNOTES

- ROM-742: Both published and estimated SPECrate®2017_int_base performance as of March 2, 2020.
  AMD EPYC 7742 (64C) score of 355 http://spec.org/cpu2017/results/res2020q1/cpu2017-20191223-20460.pdf
  AMD EPYC 7642 (48C) score of 306 http://spec.org/cpu2017/results/res2020q3/cpu2017-20200827-23775.html
  AMD EPYC 7542 (32C) score of 223 http://spec.org/cpu2017/results/res2019q4/cpu2017-20191028-19322.pdf
  AMD EPYC 7402P (24C) score of 177 http://spec.org/cpu2017/results/res2019q4/cpu2017-20191028-19326.pdf
  AMD EPYC 7302P (16C) score of 124 http://spec.org/cpu2017/results/res2019q4/cpu2017-20191125-20005.pdf
  AMD EPYC 7262 (8C) score of 68.3 http://spec.org/cpu2017/results/res2020q1/cpu2017-20191220-20437.pdf
  Intel® Xeon® Scalable 2P processors scores using the highest competitive part in the Bronze, Silver and Gold metal classes. Estimates are based on highest score 2P processor result and divided by 1.99x for conservative estimate:
  Intel Xeon Gold 6258R (28C) estimated score of 199 (derived from 2P score of 397/1.99=199) https://spec.org/cpu2017/results/res2020q3/cpu2017-20200915-23981.html
  Intel Xeon Gold 5220R (24C) estimated score of 160 (derived from 2P score of 319/1.99=160) http://spec.org/cpu2017/results/res2020q3/cpu2017-20200608-22594.html
  Intel Xeon Silver 4216 (16C) score of 87.3 http://spec.org/cpu2017/results/res2019q2/cpu2017-20190524-14372.pdf
  Intel Xeon Bronze 3206R (8C) estimated score of 30.2 (derived from 2P score of 60.1/1.99= 30.2)
  http://spec.org/cpu2017/results/res2020q2/cpu2017-20200609-22881.html
  Results may vary with production system publications. The average of all published Intel results that have a 1P and 2P corresponding number is 2.08x with the maximum being 2.3x and the minimum being 1.95x so conservatively AMD estimated using 1.99x scaling. AMD expects Intel published numbers in the near future will likely be higher. SPEC®, SPECrate® and SPEC CPU® are registered trademarks of the Standard Performance Evaluation Corporation. See www.spec.org for more information. ROM-742
- ROM-42 - Based on AMD internal testing of ANSYS FLUENT 19.1, lm6000_16m benchmark, as of July 17, 2019 of a 2P EPYC 7742 powered reference server versus a 2P Intel Xeon Platinum 8280 powered server. Results may vary.
- ROM-49 - Based on AMD internal testing of LSTC LS-DYNA R9.3.0, neon benchmark, as of July 17, 2019 of a 2P EPYC 7742 powered reference server versus a 2P Xeon Platinum 8280 powered server. Results may vary.
- ROM-56 - Based on AMD internal testing of Altair RADIOSS 2018, T10M benchmark, as of July 17, 2019 using a 2P EPYC 7742 powered reference server versus a 2P Xeon Platinum 8280 powered server. Results may vary.
- ROM-63 - Based on AMD internal testing of ESI VPS 2018.0, NEON4m benchmark, as of July 17, 2019 using a 2P EPYC 7742 powered reference server versus a 2P Xeon Platinum 8280 powered server. Results may vary.
- ROM-113
  AMD Internal testing as of 30July2019 of a 2P AMD EPYC 7742 powered reference platform versus a 2P Intel Platinum 8280 powered production server, on GROMACS version 2019.3 benchmark. Results may vary. ROM-113

ENDNOTES

MI100-04 - Calculations performed by AMD Performance Labs as of Sep 18, 2020 for the AMD Instinct™ MI100 accelerator at 1,502 MHz peak boost engine clock resulted in 184.57 TFLOPS peak theoretical half precision (FP16) and 46.14 TFLOPS peak theoretical single precision (FP32 Matrix) floating-point performance. The results calculated for Radeon Instinct™ MI50 GPU at 1,725 MHz peak engine clock resulted in 26.5 TFLOPS peak theoretical half precision (FP16) and 13.25 TFLOPS peak theoretical single precision (FP32 Matrix) floating-point performance. Server manufacturers may vary configuration offerings yielding different results. MI100-04

MI100-05 - Calculations performed by AMD Performance Labs as of Sep 18, 2020 for the AMD Instinct™ MI100 accelerator at 1,502 MHz peak boost engine clock resulted in 11.535 TFLOPS peak theoretical double precision (FP64) floating-point performance. The results calculated for Radeon Instinct™ MI50 GPU at 1,725 MHz peak engine clock resulted in 6.62 TFLOPS FP64. Server manufacturers may vary configuration offerings yielding different results. MI100-05

MI100-06 Calculations as of SEP 18th, 2020. AMD Instinct™ MI100 accelerators support PCIe® Gen4 providing up to 64 GB/s peak theoretical transport data bandwidth from CPU to GPU per card. AMD Instinct™ MI100 accelerators include three Infinity Fabric™ links providing up to 276 GB/s peak theoretical GPU to GPU or Peer-to-Peer (P2P) transport rate bandwidth performance per GPU card. Combined with PCIe Gen4 support, this provides an aggregate GPU card I/O peak bandwidth of up to 340 GB/s. Server manufacturers may vary configuration offerings yielding different results. MI100-06

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