# THE PATH TO

日本AMD エンタープライズセールス 岩佐英敏

PCクラスタコンソーシアム向け December 15<sup>TH</sup>, 2016

## OUR TWO-YEAR JOURNEY

"First and foremost, we are here to build great products through our investments in differentiated IP coupled with our design, integration, software and system capabilities."

OCTOBER 2014

## OUR FOCUS



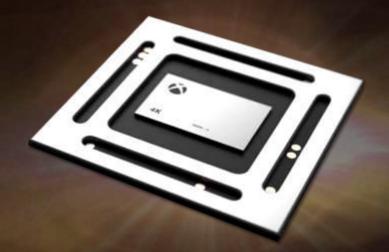


SMALLEST XBOX EVER 4K VIDEO AND HDR





4K GAMING AND VR



## PLAYSTATION 4 43 MILLION VR-READY CONSOLES



## APPLE

imac and macbook pro WITH RETINA DISPLAYS

## RADEON RX 4 8 0

## INDUSTRY FIRST PREMIUM VR STARTING AT \$199



INCREDIBLE PERFORMANCE AND FEATURES FOR PROFESSIONAL PLATFORMS





#### 7<sup>TH</sup> GENERATION A-SERIES APU

THREE STRAIGHT QUARTERS OF MOBILE APU GROWTH

RECORD ENTERPRISE SALES IN Q2 2016

Enterprise sales statement: Record sales of AMD mobile APU-based commercial systems to major corporate buyers by OEMs.



7F · AMD

1

### INNOVATIVE PARTNERSHIPS

THATIC JV TO DEVELOP SERVER SOCs FOR 2<sup>ND</sup> LARGEST SERVER MARKET

ATMP JV WITH TFME CREATES INDUSTRY-LEADING OSAT

# BEST IS YET TO COME

MOST COMPETITIVE PRODUCT LINEUP IN A DECADE

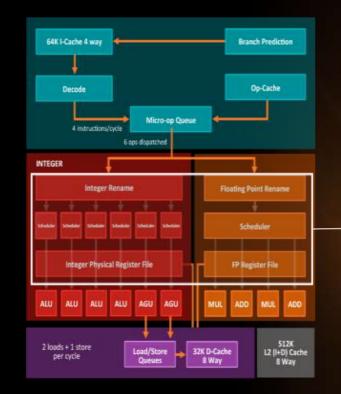
#### OUR X86 HERITAGE



## DESIGNING THE "ZEN" ENGINE

1 PERFORMANCE
2 THROUGHPUT
3 EFFICIENCY

#### DESIGNING THE ENGINE: PERFORMANCE

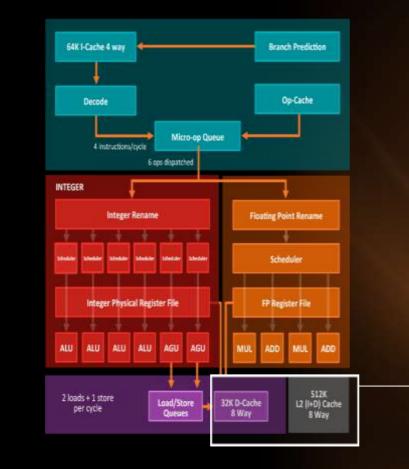


#### QUANTUM LEAP IN CORE EXECUTION CAPABILITY

- Enhanced branch prediction to select the right instructions
- Micro-op cache for efficient op issue
- 1.75X instruction scheduler window\*
- 1.5X issue width and execution resources\*
- Result: instruction level parallelism designed for dramatic gains in single-threaded performance

\*Compared to Excavator

#### DESIGNING THE ENGINE: THROUGHPUT

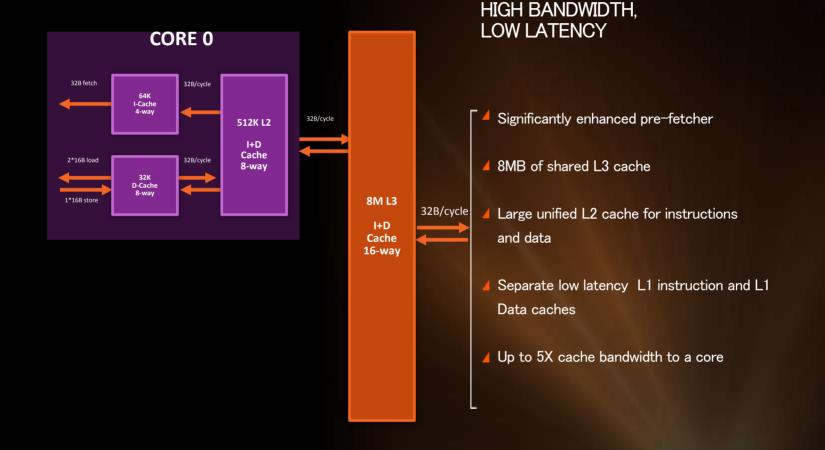


#### HIGH BANDWIDTH, LOW LATENCY

- Significantly enhanced pre-fetcher
- 8MB of shared L3 cache
- Large unified L2 cache for instructions and data
- Separate low latency L1 instruction and L1 Data caches
- Up to 5X cache bandwidth to a core



#### DESIGNING THE ENGINE: THROUGHPUT

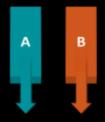


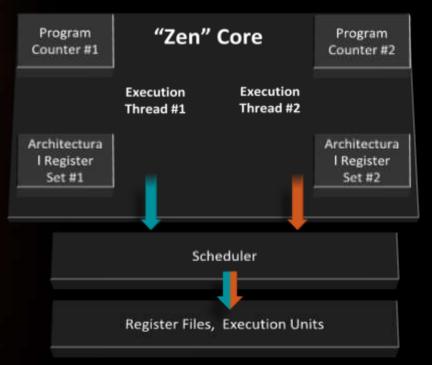
## DESIGNING THE ENGINE: THROUGHPUT

#### SIMULTANEOUS MULTI-THREADING

- Thread appears the same as an independent core to software
- High performance cores have gaps in utilization now exploited for an additional thread
- Excellent synergy with single thread more execution resources benefit both modes

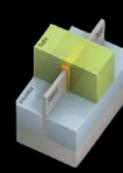
Program Threads





## DESIGNING THE ENGINE: EFFICIENCY

#### IMPROVED TRANSISTOR DENSITY & EFFICIENCY

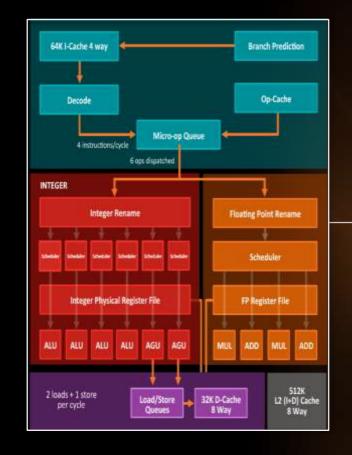


Energy-efficient 14nm FinFET design scales from client to enterprise-class products FinFET PROCESS BENEFIT

**Relative Power** 

Chart for illustrative purpos

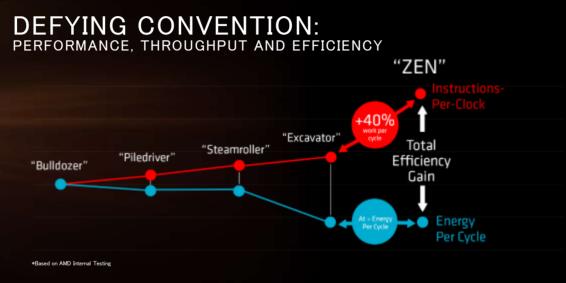
#### DESIGNING THE ENGINE: EFFICIENCY



#### LOW-POWER DESIGN METHODOLOGIES

- Aggressive clock gating with multi-level regions
- Write back L1 cache
- ▲ Large Micro-op cache
- Stack Engine
- Move elimination





#### 

Chart for illustrative purposes only





## "SUMMIT RIDGE"

- 8 CORES, 16 THREADS AM4 Platform
  - DDR4
  - PCI EXPRESS® GEN 3
  - NEXT-GEN I/O

#### AMD consortium activity

EFFORT TO BRING OPEN STANDARDS INTO THE DATACENTER

- これまでのOpen Standardへの参画
  - HSA (Heterogeneous System Architecture)
     異なるアーキテクチャのデバイス間のプログラミングモデルを提唱
  - -•GPUOpen

Open Standard platformにAMDが寄与したツールやソフトウェアを一か所でアクセスできる サイト

#### 2016年に発表したコンソーシアム

-Gen-Z

メモリーやアクセラレータへのラックスケールの接続

OpenCAPI

データセンターサーバ向けのオープンなインターフェース規格

- CCIX

複数のプロセッサアーキテクチャとアクセラレータ間のシームレスなデータ共有を狙う接続 技術

## "NAPLES" SERVER SOC



## ZEN DEMOS TODAY



## ZEN CORE MARKET ROLLOUT



## THE LAST

Released Game-Changing Polaris GPU Architecture and 7<sup>th</sup> Gen APUs Ramped Game Consoles and New Semi-Custom Business Announced Two New JVs in China

## THE NEXT 12 MONTHS

GPU Market Share Gains with Polaris and New Vega Architecture Return to Growth In PCs with "Zen" Re-Enter Highly-Profitable x86 Server Market with "Naples" Ramp New Semi-Custom Business

## BEST IS YET TO COME

## ご静聴ありがとうございました。

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