Hybrid Computing for High-Throughput Bioinformatics

THE WORLD'S FIRST HYBRID-CORE COMPUTER.

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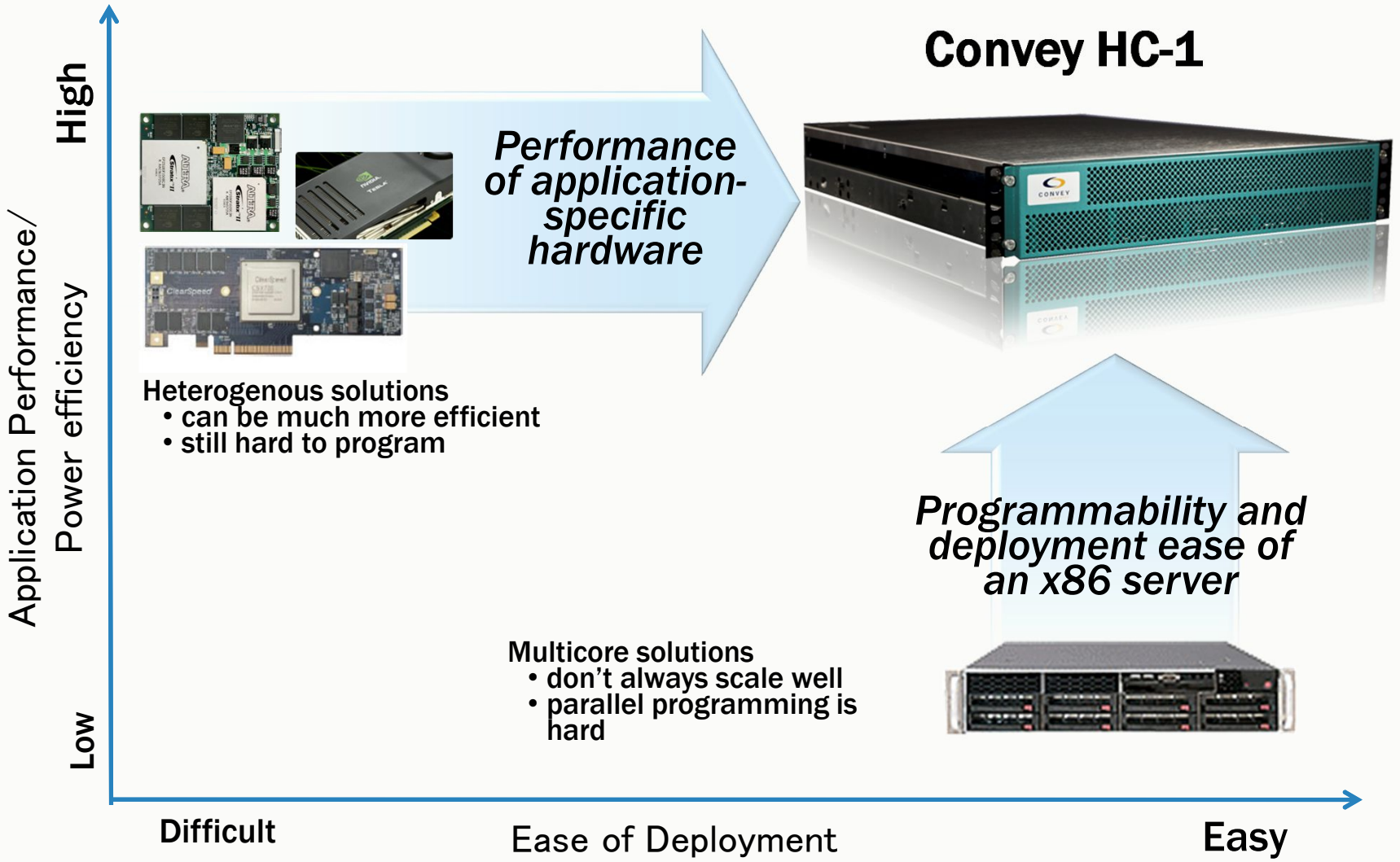
Hybrid-core Computing



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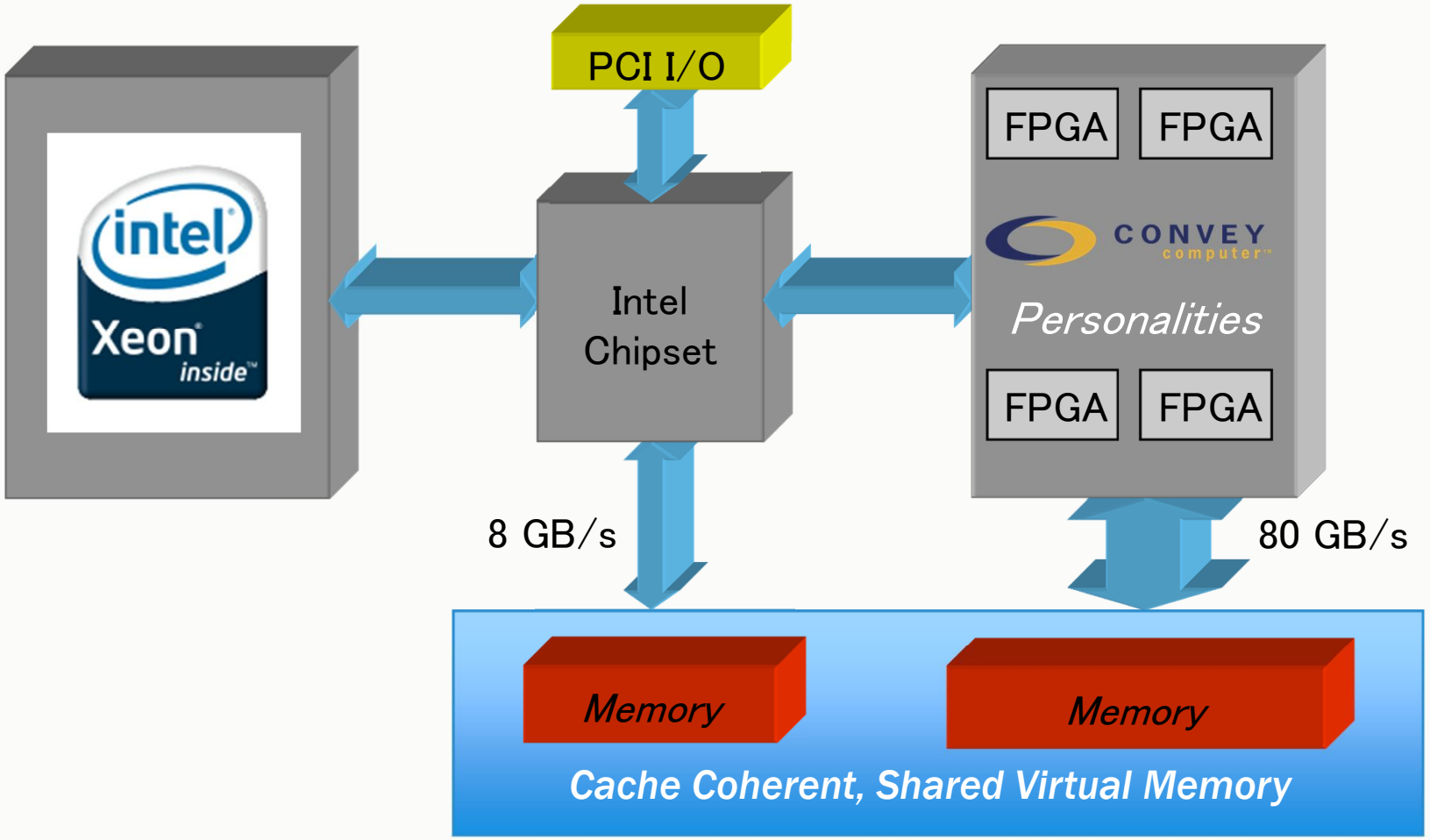
SYSTEM ARCHITECTURE

HC-1 Hardware



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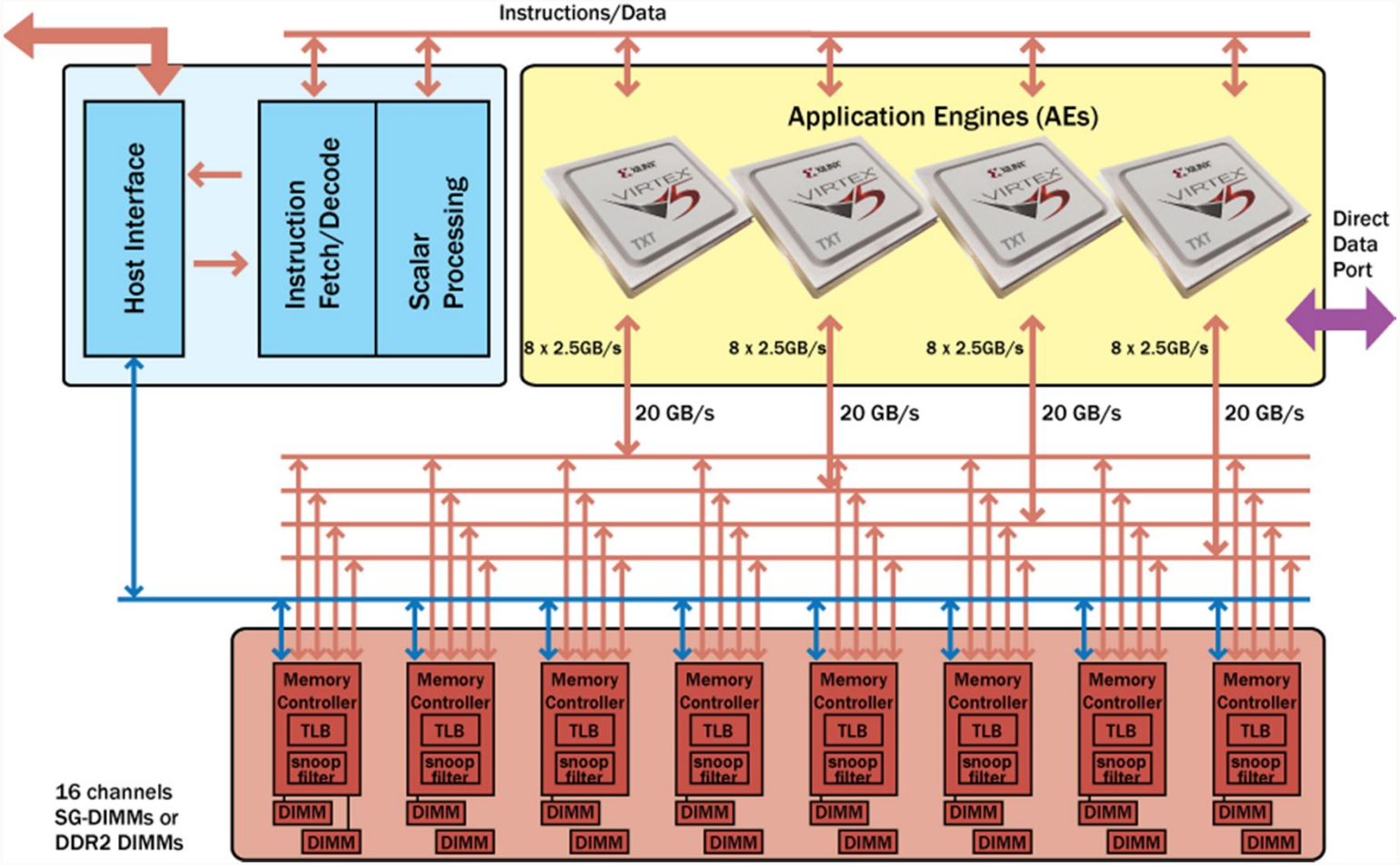
Memory Subsystem

- Optimized for 64-bit accesses; 80 GB/sec peak
- Automatically maintains coherency without impacting AE performance



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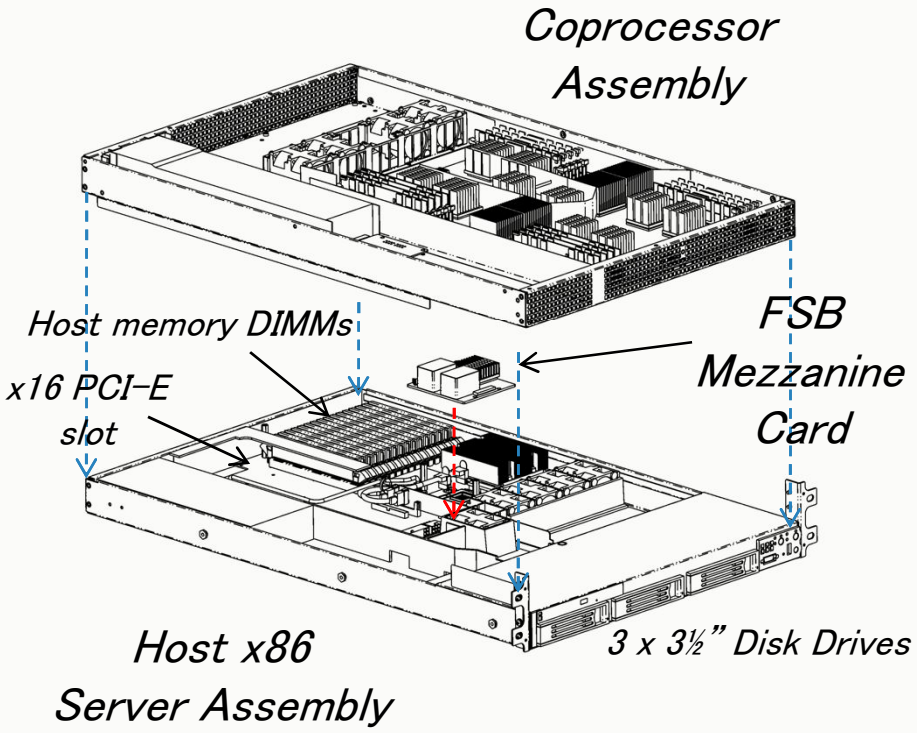
HC-1 Hardware



- **2U enclosure:**
  - Top half of 2U platform contains the coprocessor
  - Bottom half contains Intel motherboard

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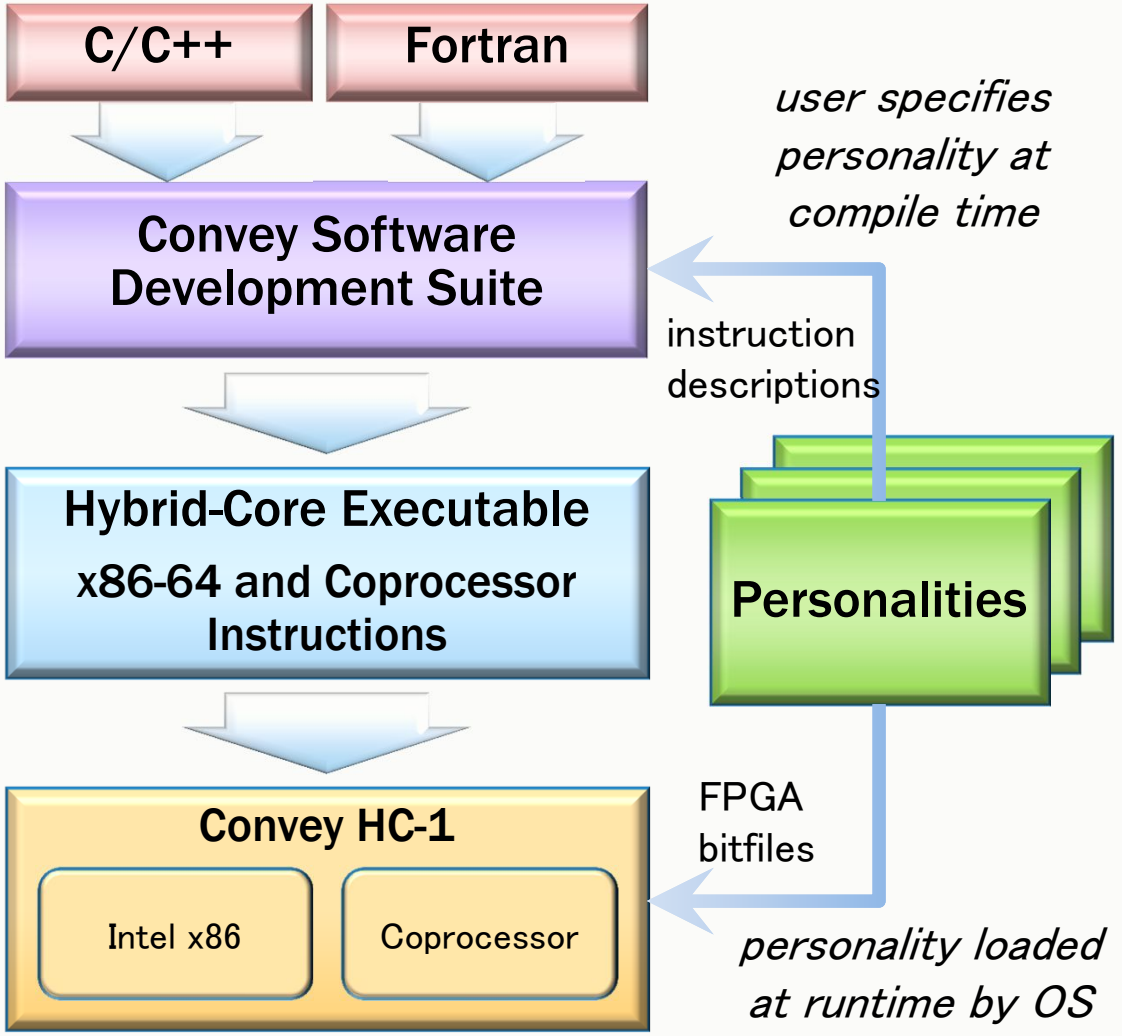
Using Personalities

- Personalities are reloadable instruction sets
- Compiler generates x86 and coprocessor instructions
- ANSI standard C/C++ & Fortran
- Executable runs on x86 nodes or Convey Hybrid-Core nodes



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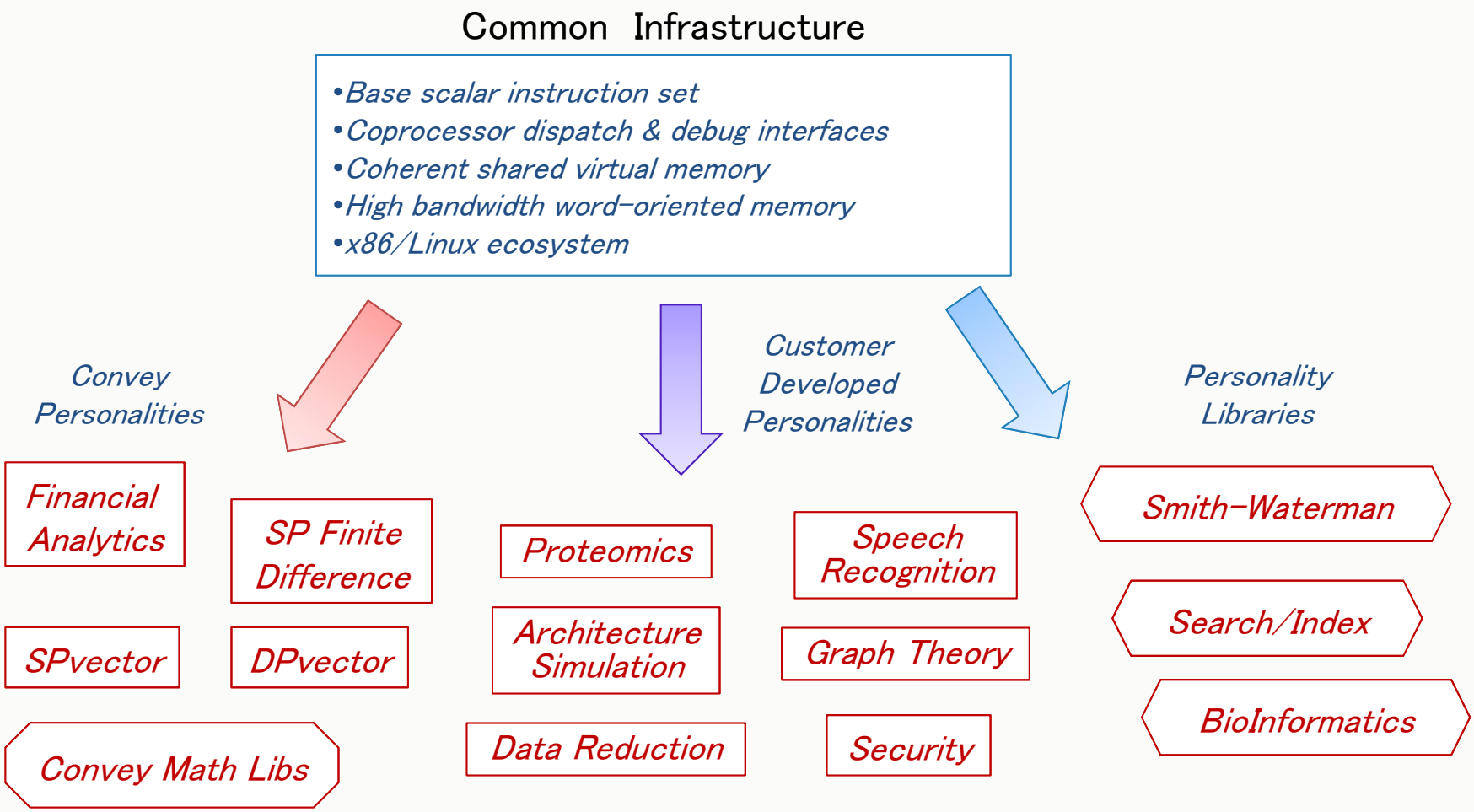
Personalities: Application Specific Architectures



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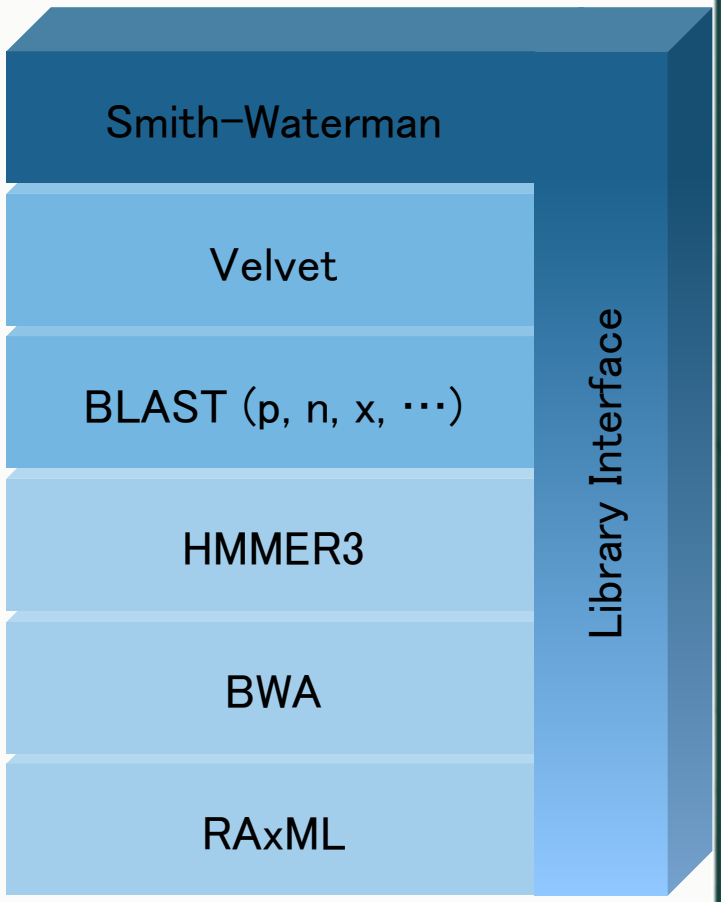
SEQUENCING AND ALIGNMENT SUITE

Sequencing and Alignment Suite

- **Smith-Waterman**
  - Nucleotides and Proteins
  - Linear scoring now
  - Soon table & affine
- **On the Roadmap**
  - Velvet
  - BLAST (p, n, x, …)
- **Likely future applications (customer prioritized)**
  - HMMER3
  - BWA
  - RAxML



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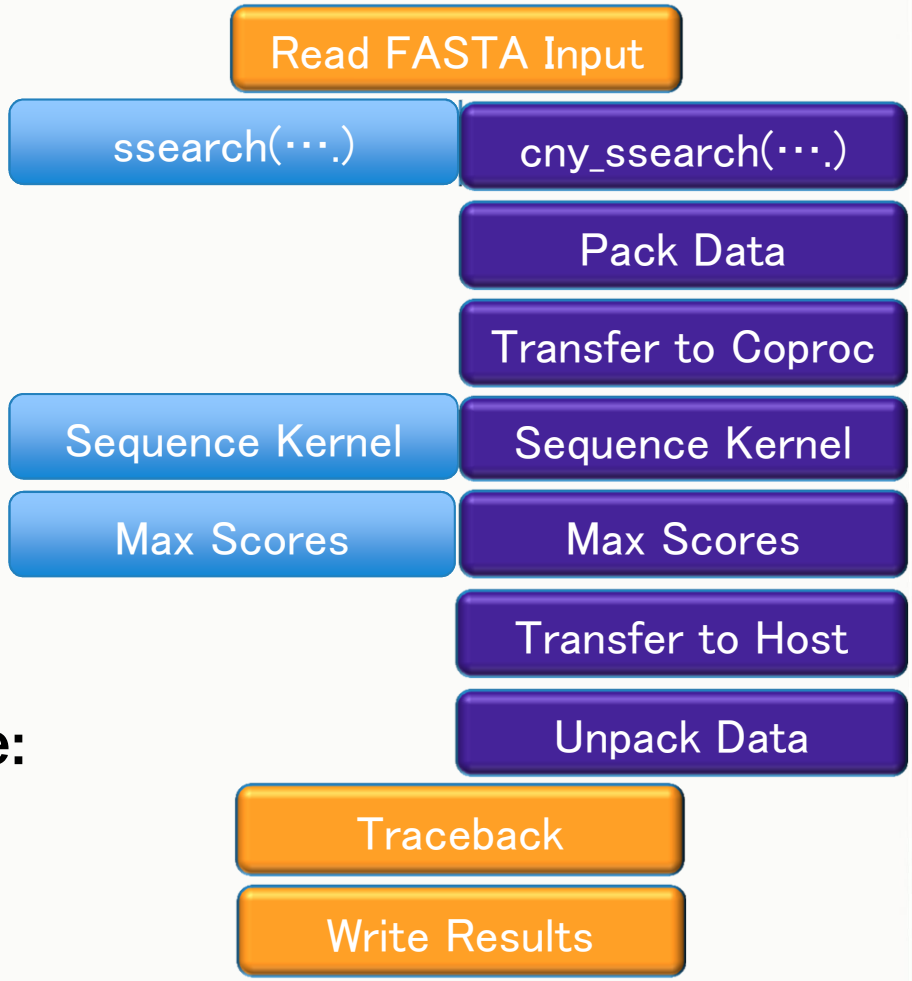
Convey Smith-Waterman Personality Library

- **Basic**
  - single function call
  - handles all memory access, dispatch, cleanup
- **Synchronous Configurable**
  - several functions
  - myriad options to configure sequence searches
  - pack multiple searches into search streams
- **Asynchronous Configurable:**
  - in order to gain maximal performance



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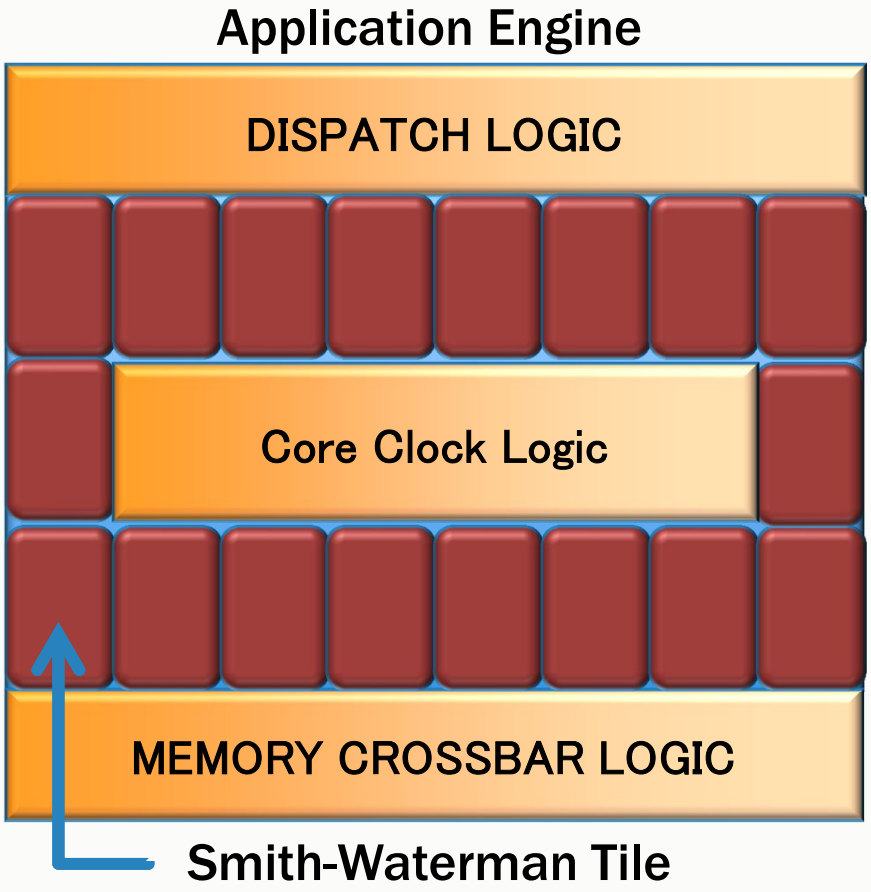
Smith-Waterman Personality

- **18 tiles of S-W on each AE**
- **Each tile**
  - Systolic array unrolled in HW
  - 64 input cells / clock cycle
  - Clock @ 150Mhz
  - Generates 64 results / clock
- **Join two tiles for input sequences length 128**
- **Database > 1 B characters**
- **Data is packed**
  - 8 elements in each 64bit LOAD and STORE



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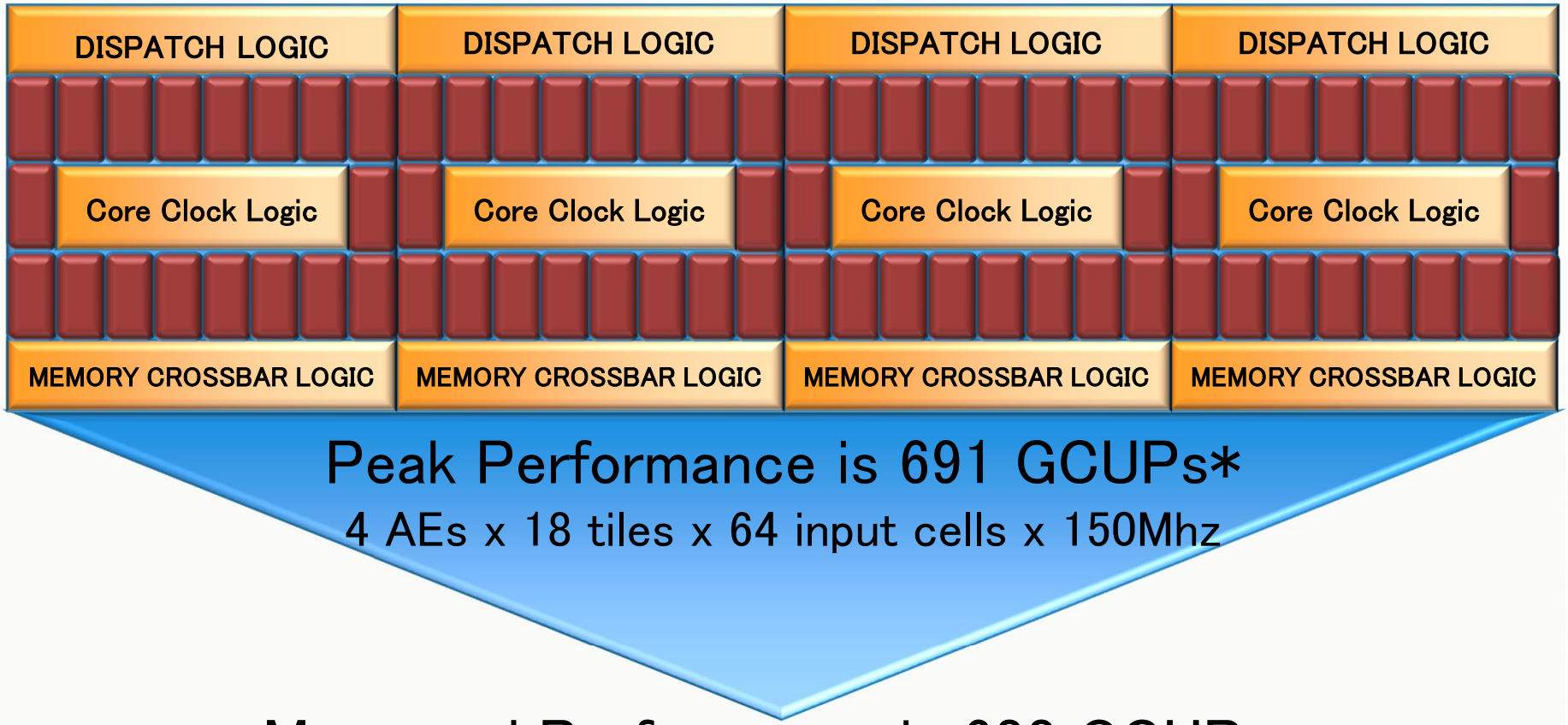
Aggregate Performance



Peak Performance is 691 GCUPs*

4 AEs x 18 tiles x 64 input cells x 150Mhz

Measured Performance is 688 GCUPs*

Core kernel 99.6% efficient

*GCUPs = billions of cell updates per second

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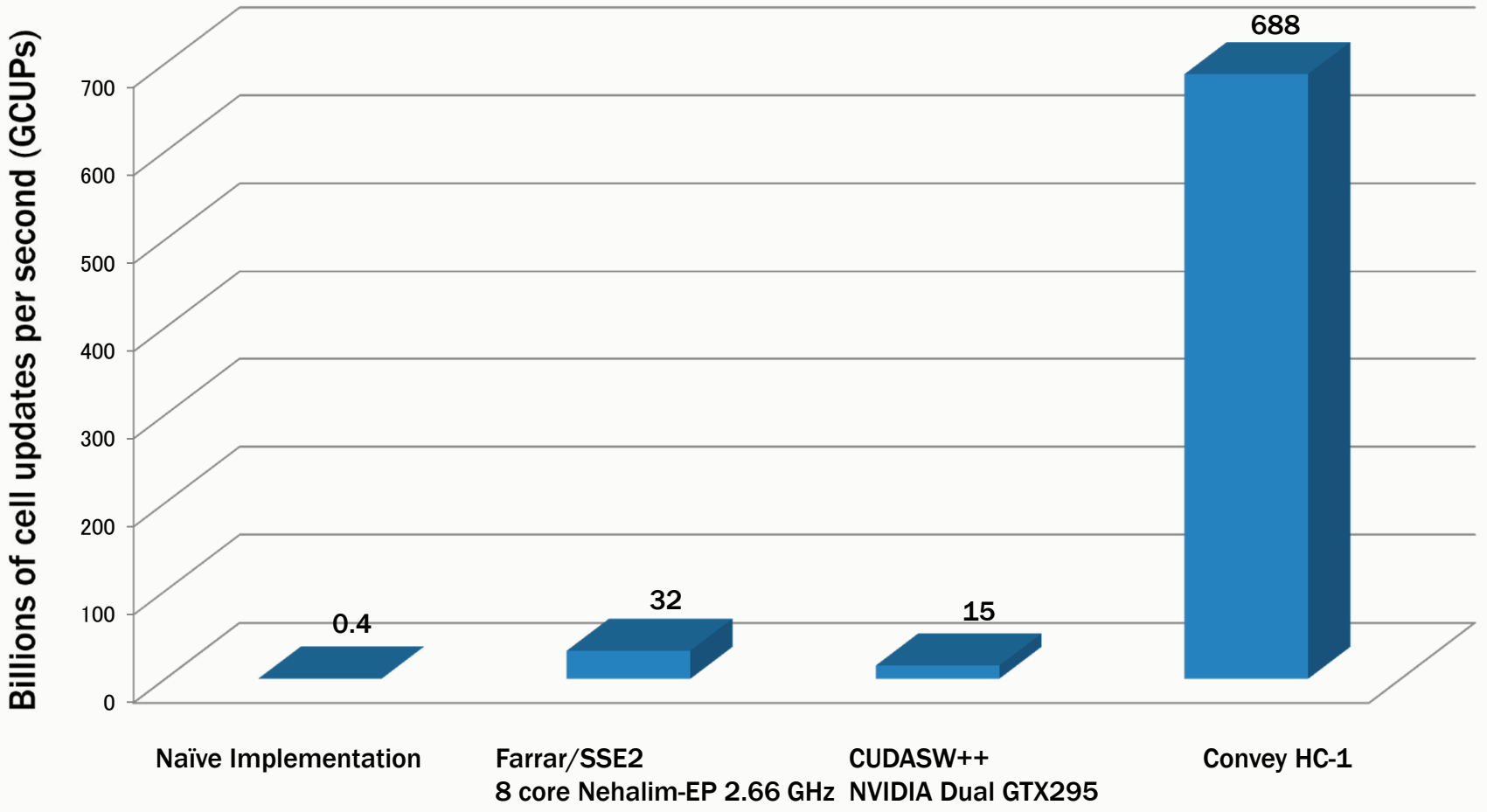
Smith-Waterman Performance



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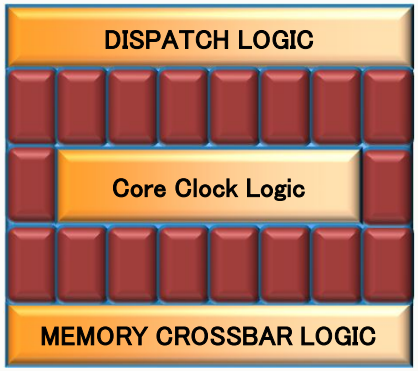
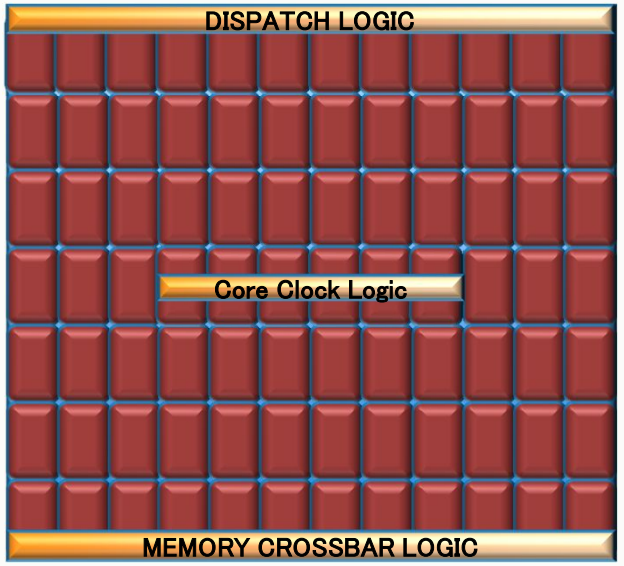
Smith-Waterman Example

- **Smith-Waterman Linear Search**
  - Algorithm is “tiled” across each application engine
  - HC-1: 72 tiles
  - HC-1^{ex}: 168 tiles
- **Kernel 99.5% efficient**

HC-1



HC-1^{ex}



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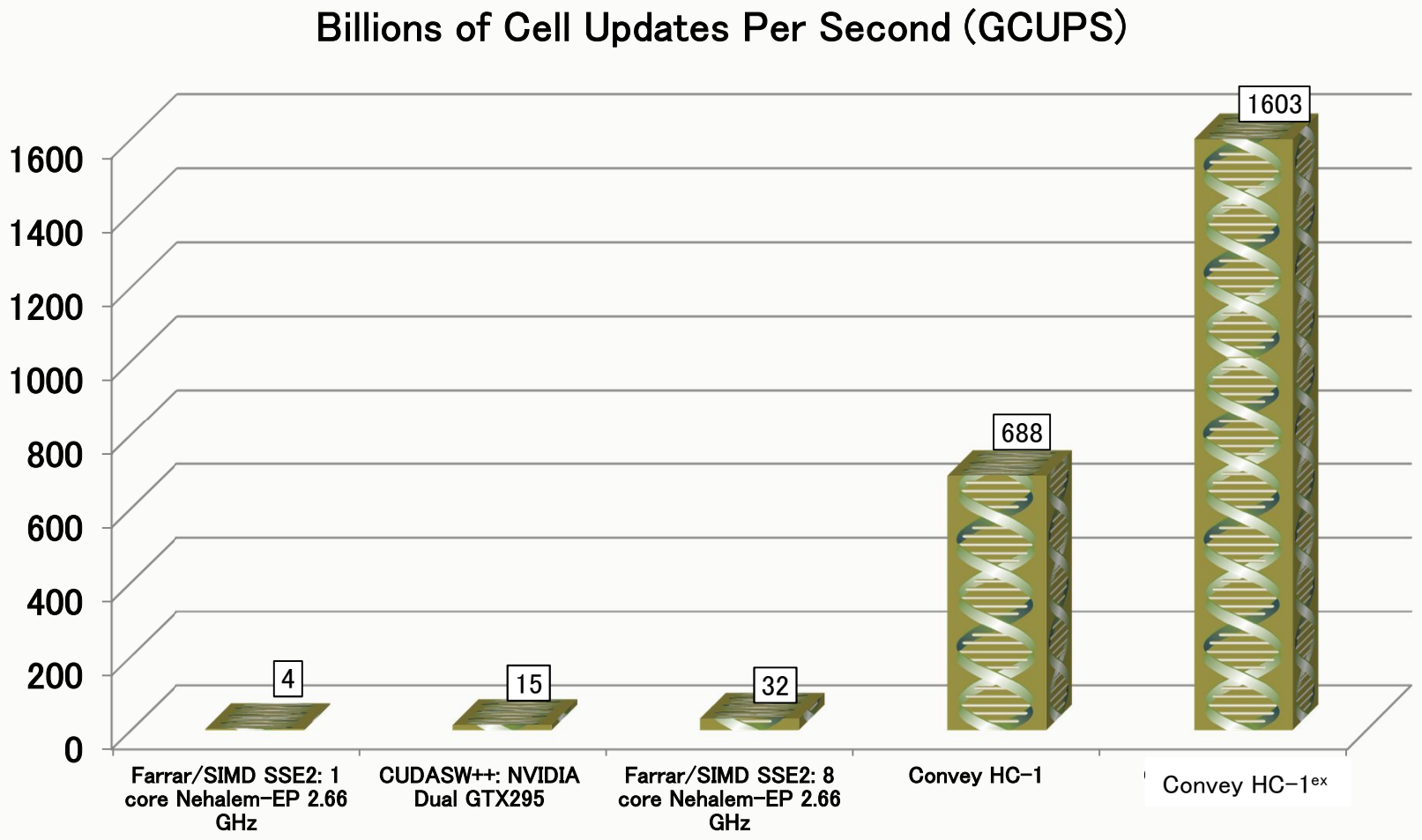
Extreme Performance



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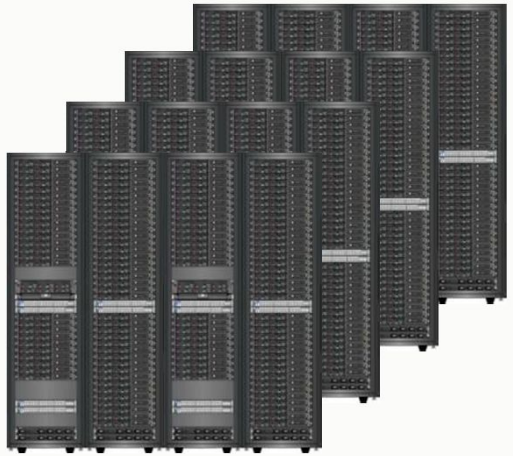
Exceptional Energy Efficiency

One rack of Convey HC-1 servers can replace as many as 10 racks of commodity servers.[2]

- Reduces floor space by 86%
- Reduces datacenter watts by 91%.
- Reduces 3-year TCO by 75%.
- Reduces 3-year TCO with power rebate 82%

One rack of Convey HC-1^{ex} servers achieves even greater energy efficiency. One rack can replace as many as 16 racks of commodity servers.[3]

- Reduces floor space by 94%
- Reduces datacenter watts by 93%.
- Reduces 3-year TCO by 90%.
- Reduces 3-year TCO with power rebate 94%



[2]"Convey Computer™ Corporation Ships to First Customer: University of California, San Diego," June 23, 2009.
[3]Based on University of California, San Diego analysis and internal Convey benchmarks

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